4. CMOS 2 input multiplexer:

In the complemantary mos tranisistor is a 2 iputs I_0 and I_1. give the output is F.

2x1 Mux

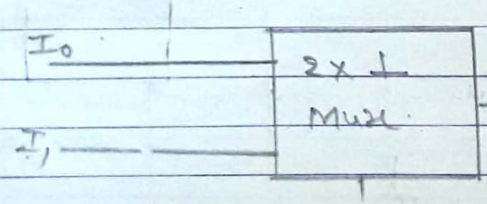


fig:(a) Symbol of 2x1 mux

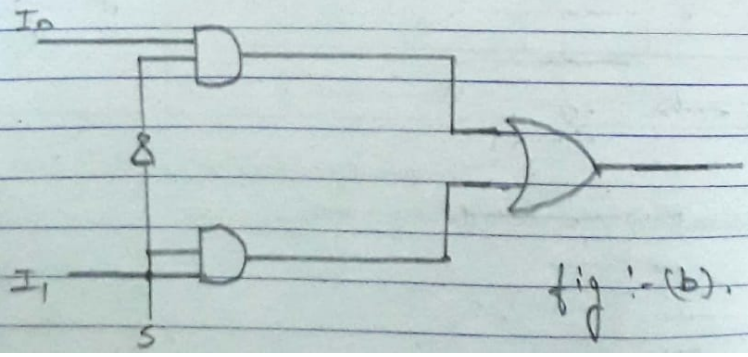


fig:-(b). diagram of 2x1 mux cmos

$F = I_0 \bar{S} + I_1 S$

$F = \bar{F} = \overline{I_0 \bar{S} + I_1 S}$

$F = \overline{I_0 \bar{S}} \cdot \overline{I_1 S}$

$F = (\bar{I}_0 + S) \cdot (\bar{I}_1 + \bar{S}_1)$ — (1)

or equation (1) do draw the CMOS 2x1 MUX diagram.

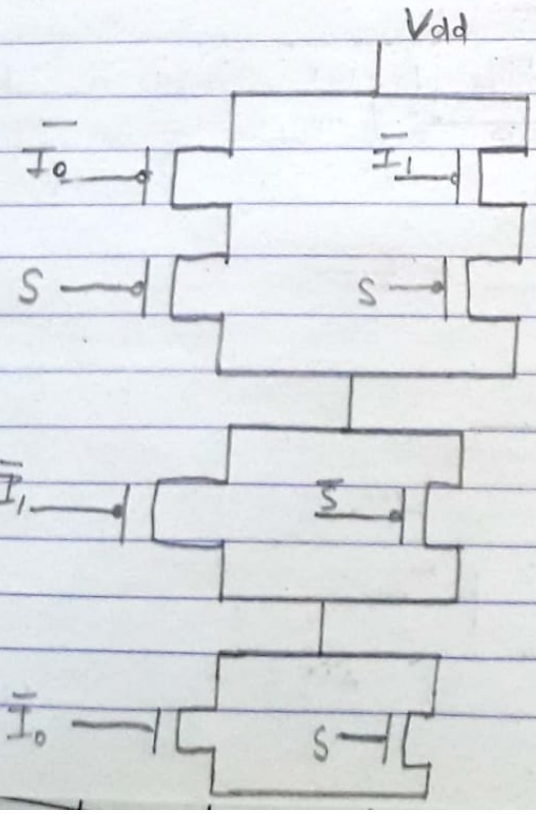


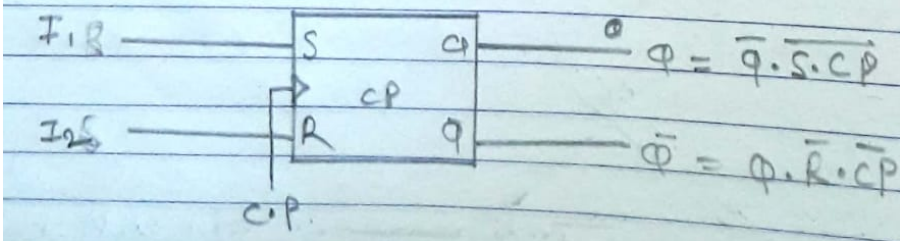
fig (c) CMOS 2x1 Multiplexer diagram

5.1. Memory latch cmos logic circuit.

In the cmos latching the ~~transi~~ data in transmission gate and drain the latch the feedback and hold the data at this point. The cmos latching is more types Flip-Flop.

1 RS Flip Flop.
2 T- Flip Flop
3 D- Flip Flop.

1. R-S Flip Flop. :- In the fig(a) shows a R-S F/F and Table 1. is shows a Table of a R-S flip flop

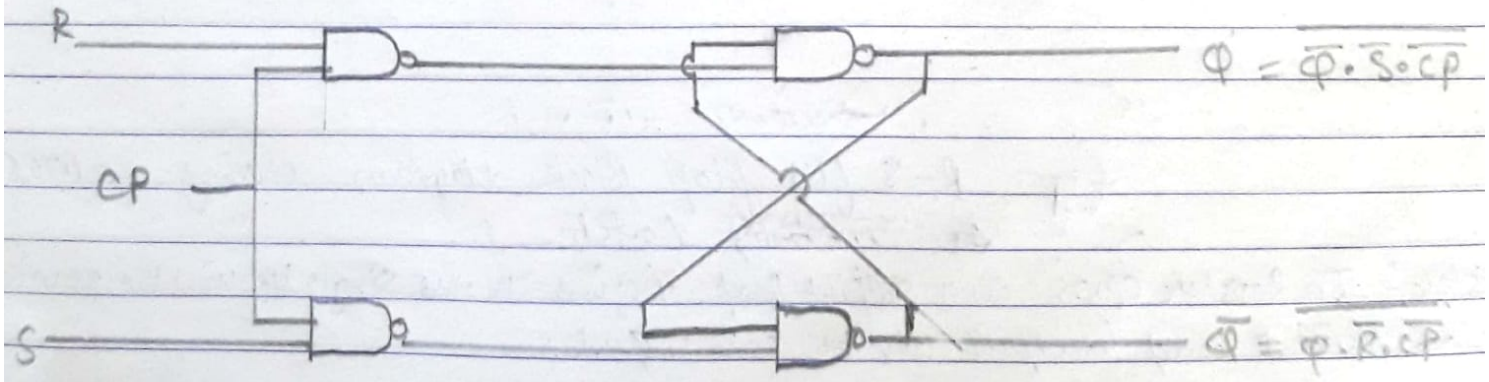


fig(a). R-S flip flop.

Bit.	Bits	Φ_{m+1}
0	0	Φ_m
0	1	0
1	0	1
1	1	Indeterminate

Table 1. R-S filp flop table.

R-S filp flop using nand gate. Block diagram.



fig(c) - Block diagram of R-S F/F using NAND gates.

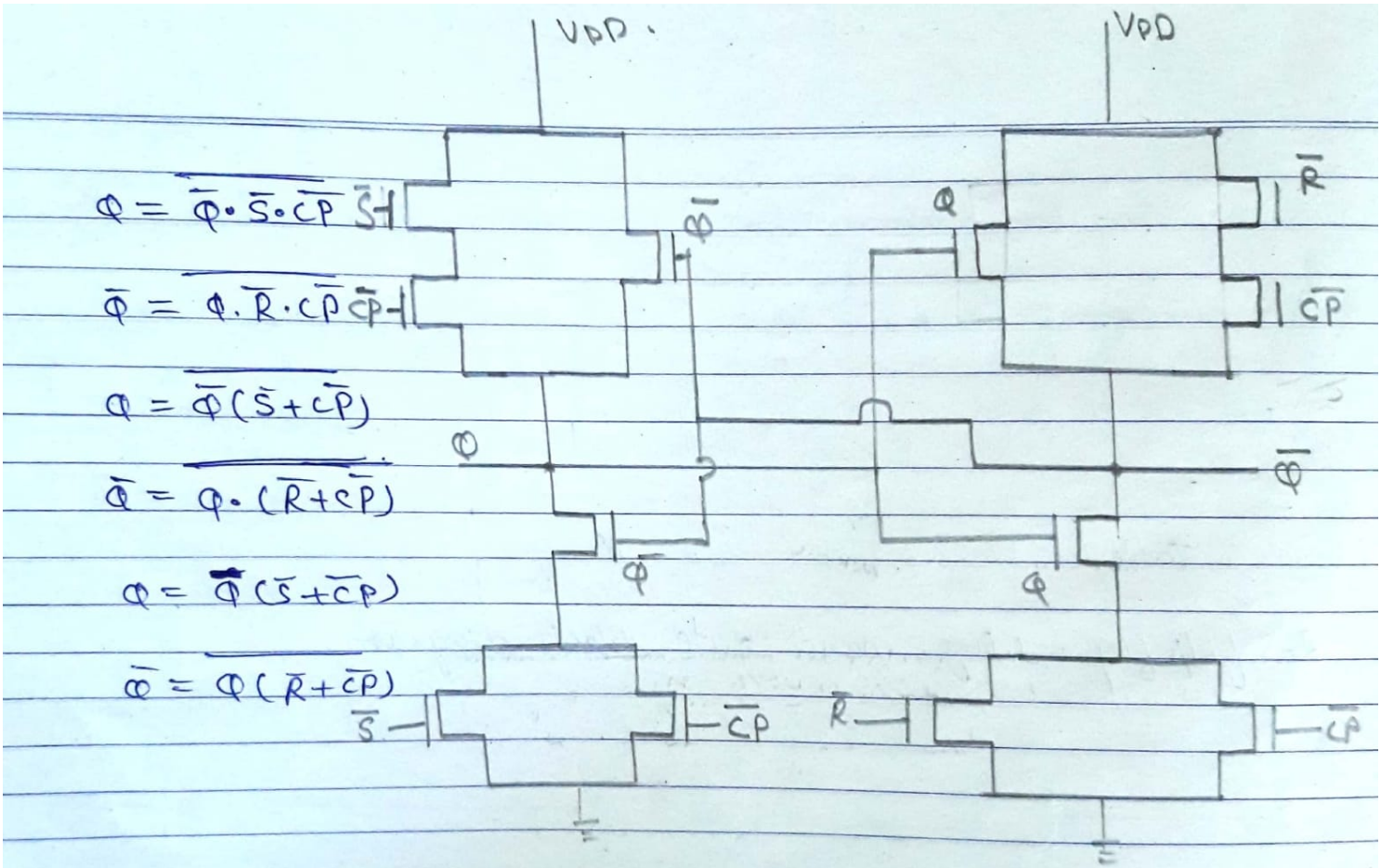


fig. R-S flip flop Block diagram using cMOS
memory Latch

Resistele:- In Resister CMOS is a ~~Shift~~ Flip flop. is give. In the single i/p will be gowith clock pluse F and output will be same give.

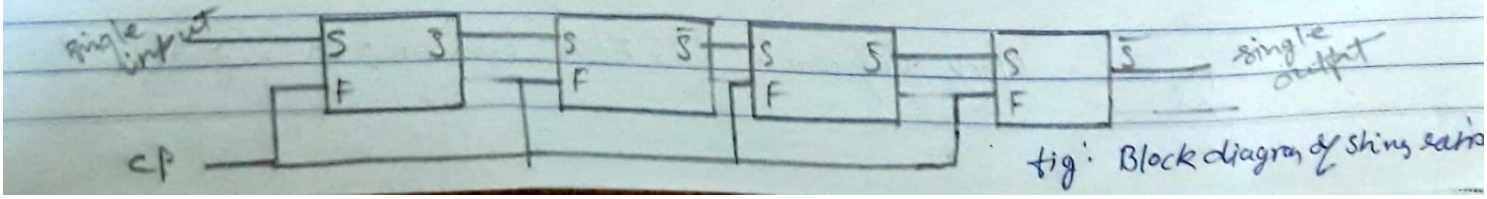


fig: Block diagram of shing sati

classification:
1. Single input Parrell output (SIPO)
2. Single input serin output (SISO)
3. Single output Parrell input (SoPI)
4. Single output serin input. (SOSI).

hw 2. Enhancement mode transistor action :-

The fig (a) will be show. of a enhancement mode MOS transistor action. i) when the $V_{GS} > V_{th}$ the enhancement will be established and the $V_{DS} = 0$ the drain and source between the current will be Zero.

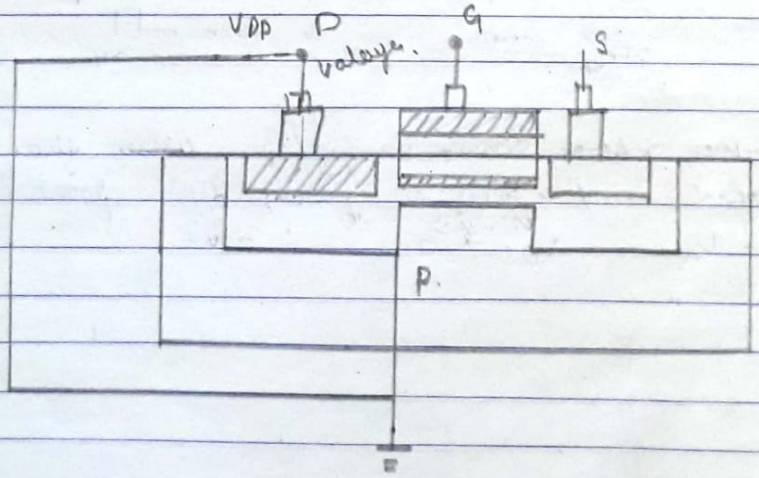
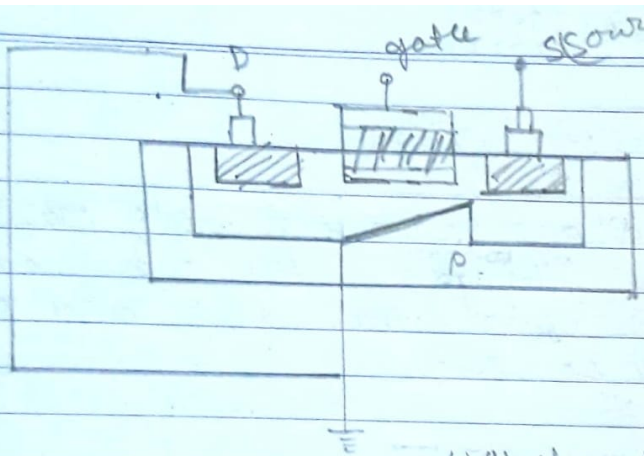


fig (a) when $V_{GS} > V_{th}$, $V_{DS} = 0$.

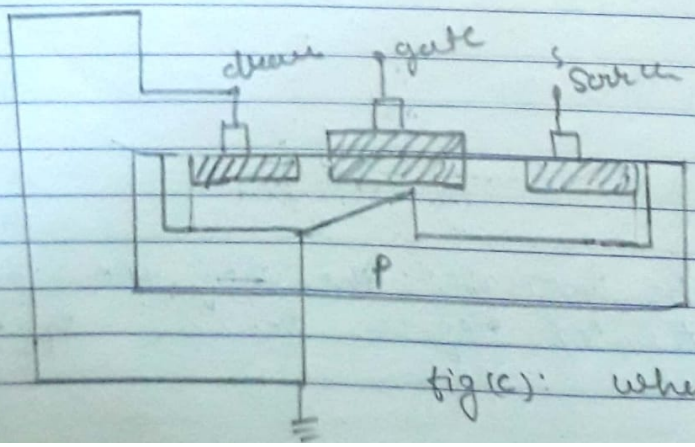
ii) when the V_{GS} V_{DS} will be increased the then the region will be non-saturated region. $V_{GS} > V_{th}$ $V_{DS} < V_{GS} - V_{th}$
$V_{DS} \neq 0$.



fig(b) When $V_{GS} - V_{th} > V_{DS}$, $V_{GS} > V_{th}$

i) When the $V_{DS} > V_{GS} - V_{th}$ ~~then~~ shown in fig(c). ~~the~~ than the given region will be saturated and give a 'pinch off' point in the.

$V_{DS} > V_{GS} - V_{th}$, $V_{DS} \neq 0$

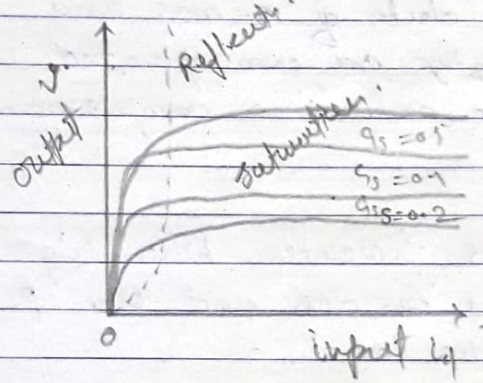


fig(c): When $V_{GS} > V_{th}$, $V_{DS} > V_{GS} - V_{th}$

Characteristics of enchanchment mode transistor action.

i) $I_d - V$ characteristics :-

$$I_d = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{N}\right) V_{ds}^2$$



ii) Pinch off Behaviour :-

In the pinch of behaviour the $V_{ds} > V_{GS} - V_{th}$ then the $x \leq L$ to give a saturated region and this situation calls a 'Pinch off'.

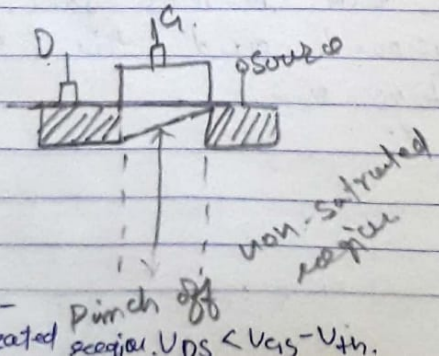


fig: Non-Saturated region. $V_{DS} < V_{GS} - V_{th}$.

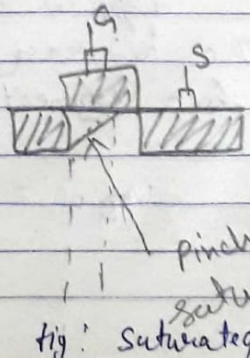


fig: Saturated region $V_{DS} > V_{GS} - V_{th}$

Ans. 3. CMOS Inverter :- In the ~~transmission~~ the enchancement data of n-mos and the enchancement data of P-Mos transistor are ~~com~~ operated in a coplemantary. This process are called a complemantry MOS (CMOS) inverter

working :-
In the CMOS inverter. When high voltage than the n-mos transisotor are ~~on~~ ON and the P- MOS transisotor are ~~act~~ while act the load.

When the low voltage than the P-Mos transistor are on. and the N-Mos transistor are while a act of the load.

circuit operation: In the CMOS transistor. i/p voltage is applied the P-Mos and N-Mos. gate V_{gs}. The N-Mos is a ground and the P-Mos is a connect to a voltage V_{DD}.

$$V_{gs_1 n} = V_{ip}$$

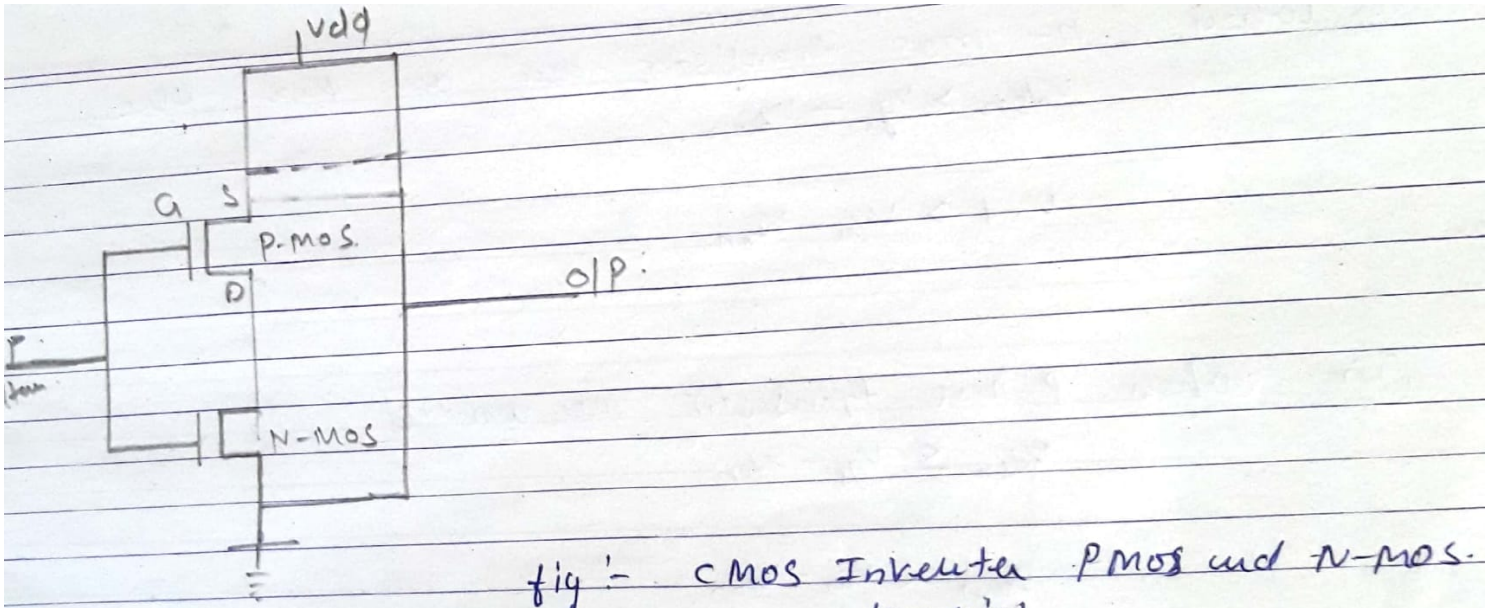


fig :- CMOS Inverter PMOS and N-MOS transistor.

$V_{ds,n} = V_{out}$

$V_{gs}P = V_{gp} - V_{sp}$

$V_{gs,p} = V_{in} - V_{out}$

$V_{gs,p} = -(V_{out} - V_{in})$

$V_{gs,p} = -(V_{dd} - V_{in})$

$V_{ds}p = -(V_{dd} - V_{out})$.

(i) When n- mos transistor are on. then the

$V_{dsn} \geq V_{gs} - V_{ton}$.

$V_{out} > V_{in} - V_{ton}$

(ii) When p-mos transistor are worked

$V_{dsn} \leq V_{gs} - V_{ton}$

$V_{out} < V_{in} - V_{ton}$.

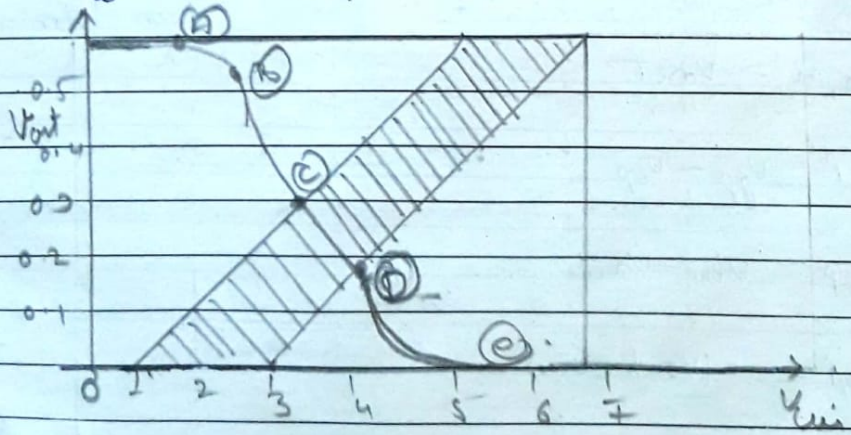


fig:- graphically representation of a cmos inverter