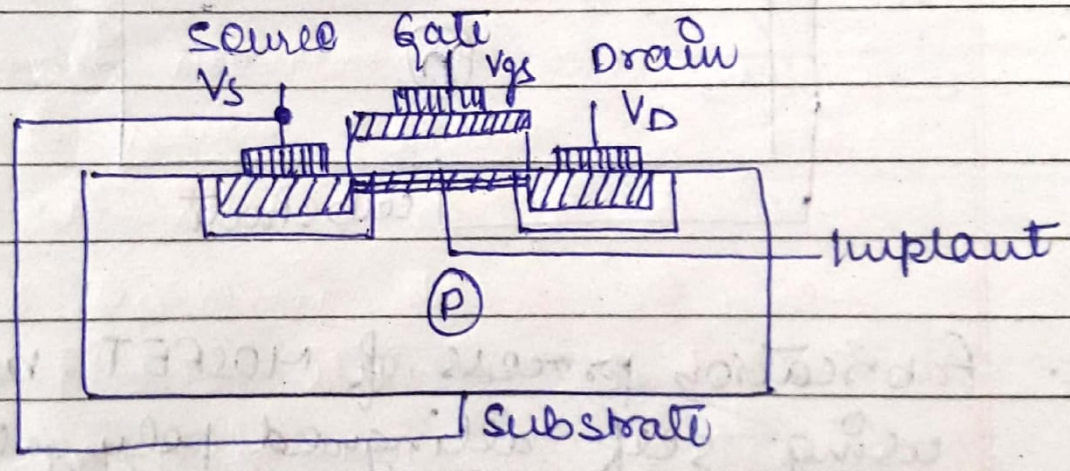
1. Explain the structure and operation of MOS Transistors?

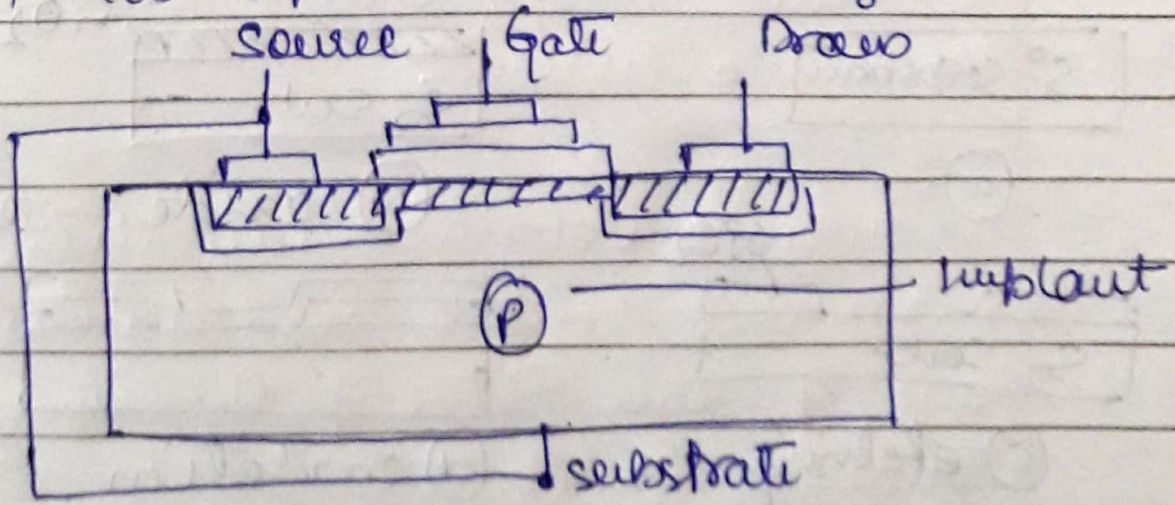
MOS Transistor are also called as MOSFET's. They can be broadly classified into four categories-

n-type depletion
p-type depletion
n-type enhancement
p-type enhancement.

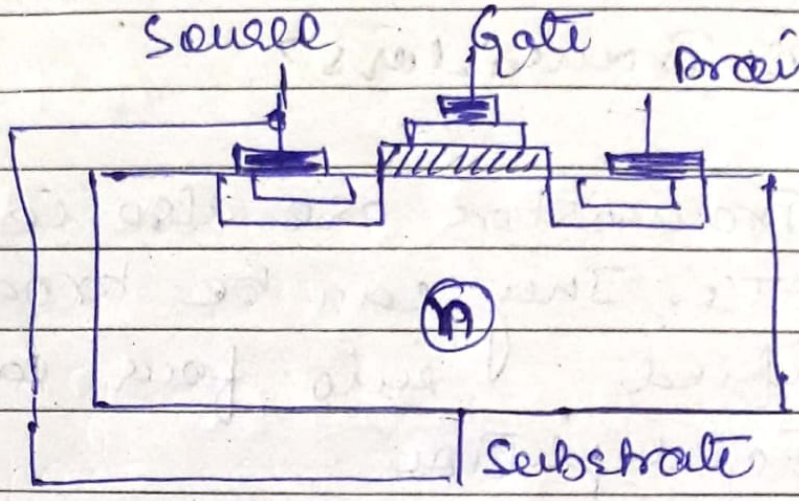
n-MOS enhancement mode



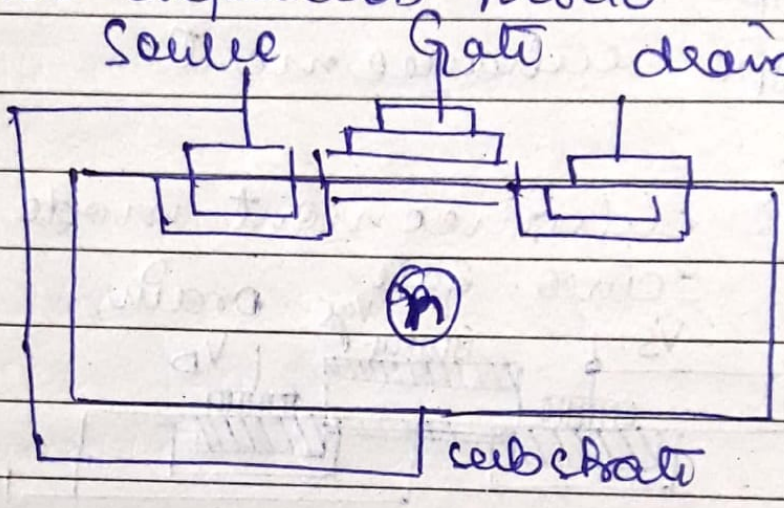
n-MOS depletion mode.



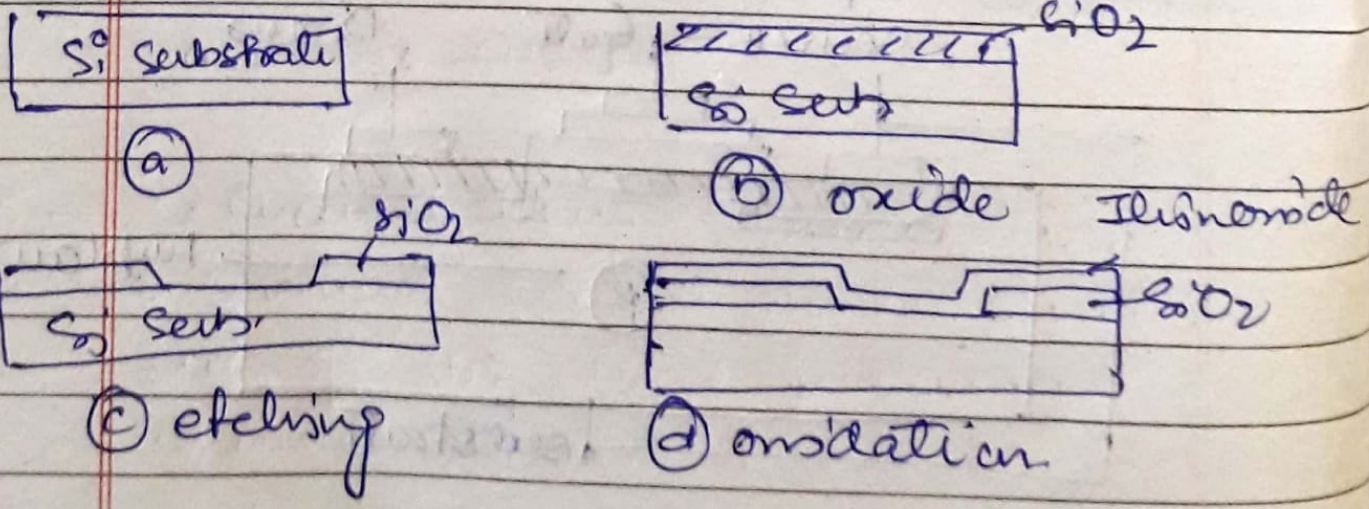
p mos enhancement mode



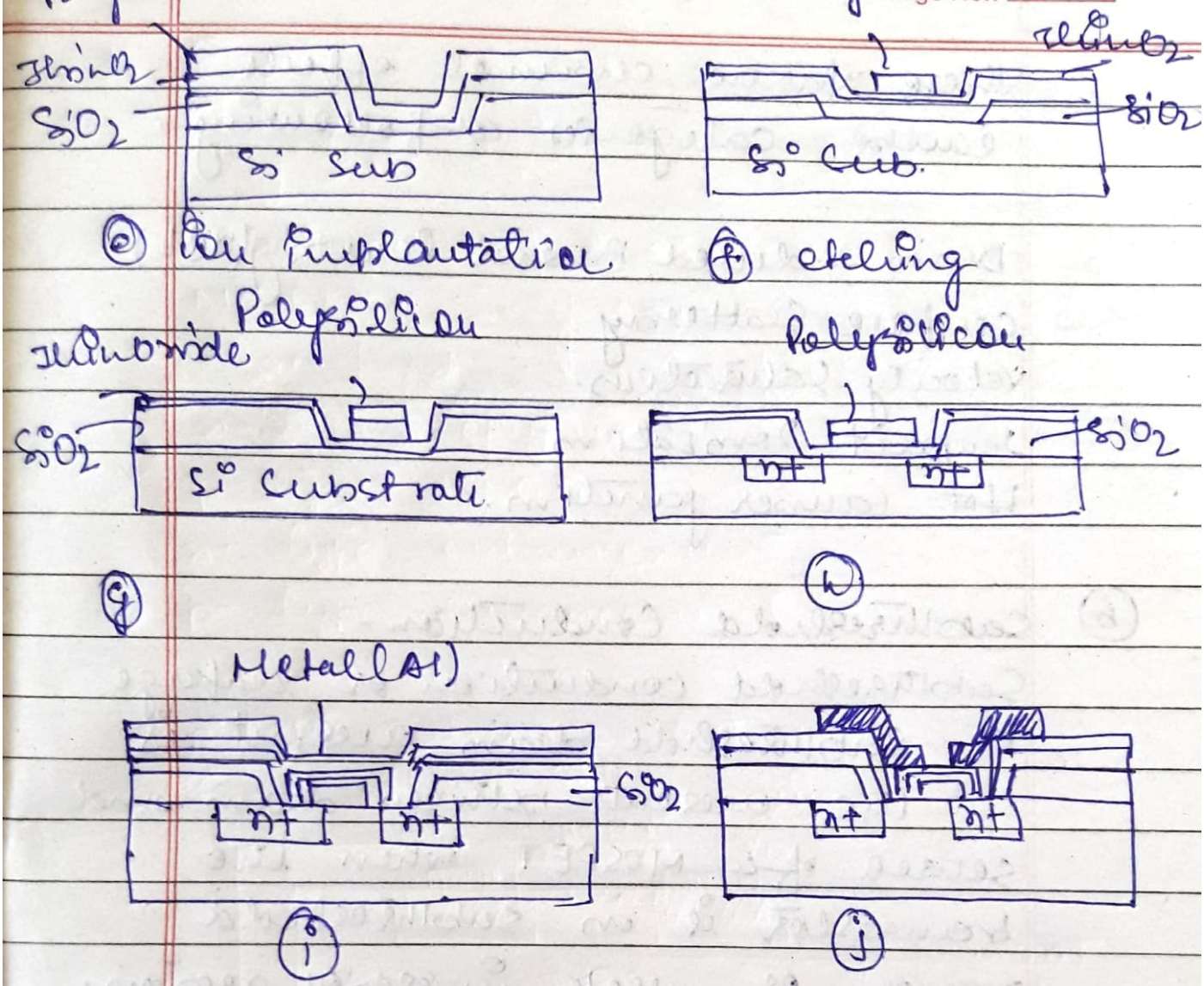
p-MOS depletion mode



2. Fabrication process of MOSFET by using self allinged poly gate technology?



Date __/__/____ Page No.:



(a) Ion Implantation (b) etching (c) (d) (e) (f)

4. Discuss the following high order effects in MOSFET-

(a) Narrow channel Effect-

The main drives for reducing size of transistors is their lengths, increasing speed and reducing cost. When you make circuits smaller, their capacitances reduces. Thereby increasing operating speed. So, Narrow channel effect created.

These Narrow channel effects cause categories as following-

Drain Induced Barrier lowering(DIBL)
Surface Scattering
Velocity Saturation.
Impact Ionization
Hot Carrier generation.

(b) Subthreshold Conduction-
Subthreshold conduction or leakage or subthreshold drain current is the current between drain and source of a MOSFET when the transistor is in subthreshold region. or weak inversion region. In digital circuits, subthreshold conduction is generally viewed as a parasitic leakage or a state that would ideally have no current.

5. S-channel length modulation-
S-channel length modulation is one of the types of Narrow channel effect.

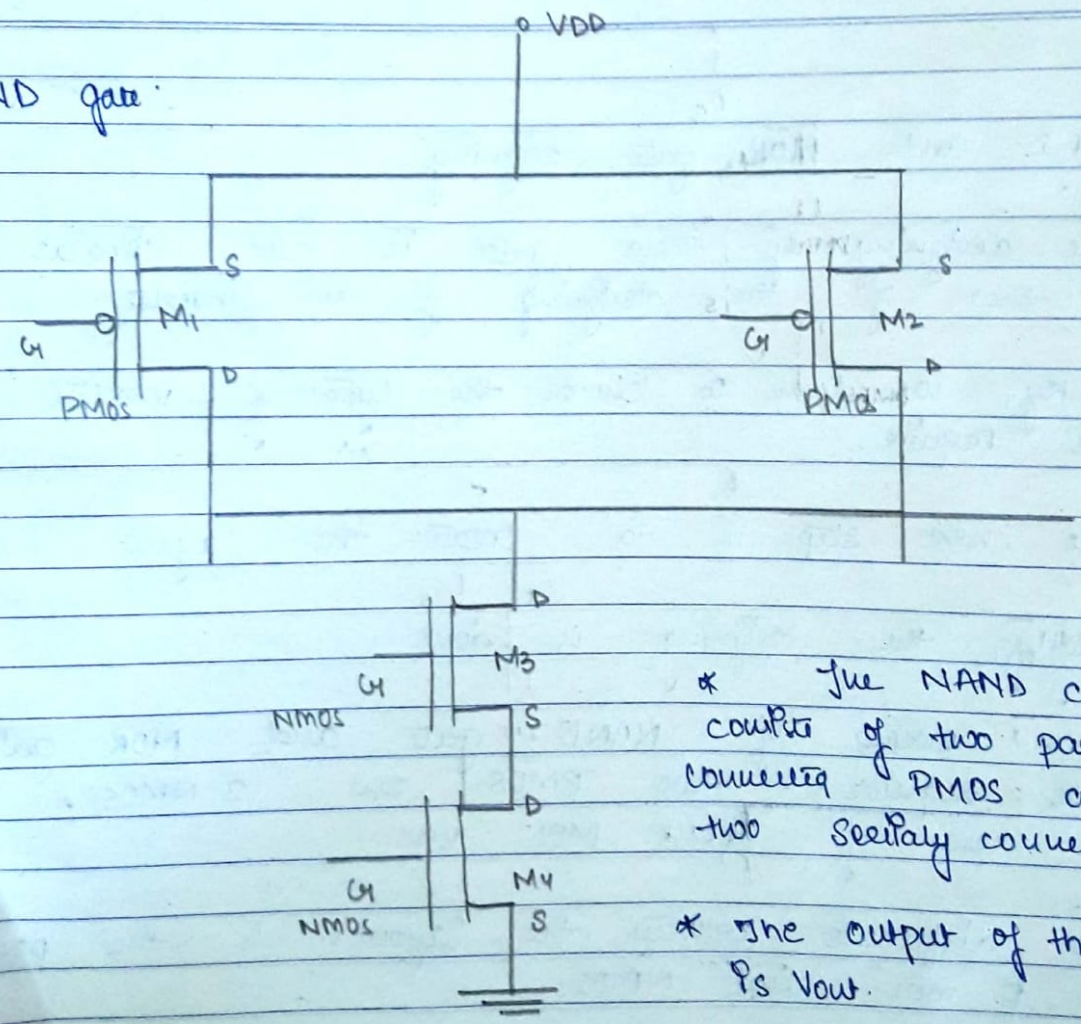
channel length modulation is a shortening of the length of the inverted channel region with increase in drain bias for large drain biases. The result of CLM is an increase in current with drain bias and reduction of output resistances.

Answer 3.

(a) NAND and NOR gate designing.

* The designing of these gates is just similar to that of the designing of an inverter
* Firstly, we have to choose the type of inverter we require
* The next step is to create the layout
* Finally, the designing is done.
* The making of NAND gate and NOR gate both require two PMOS and 2 NMOS ie use of four MOS each.
* The difference between the layout's is the positioning of P mos and NMOS.

① NAND gate.



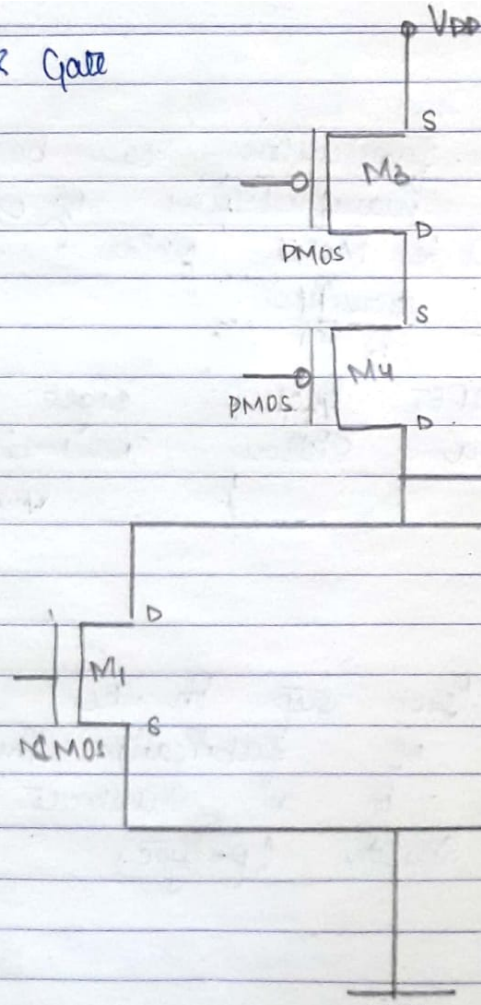
* The NAND gate consist of two parallely connected PMOS and two serially connected NMOS.

* The output of the gate is Vout.

* VDD is connected by source of two PMOS

* Ground is connected by two serial NMOS.

② NOR Gate



* The layout / design of a NOR Gate is shown in the figure.
* It consists of 4MOS i.e 2NMOS and 2PMOS.
* The two PMOS are connected serially
* And, the two NMOS are connected parallelly
* The serially connected PMOS are directly connected to VDD.
* The parallelly connected NMOS are connected to Gnd by their Source.

Answer:

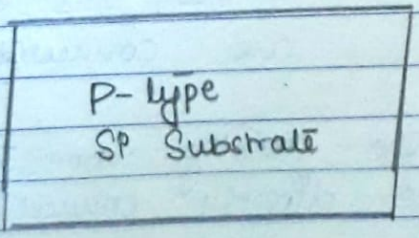
(b). Fabrication of MOSFET - fabrication can be said as a process of manufacturing of or making of a mosfet ie Metal Oxide semiconductor field effect transistor.

The fabrication of a MOSFET includes eight steps starting from a Silicon Substrate to a MOSFET

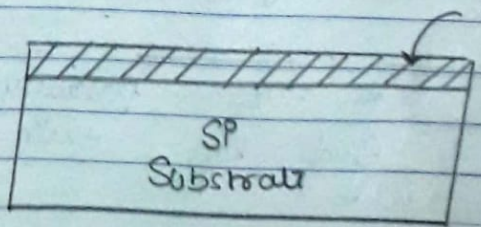
Steps

Step 1

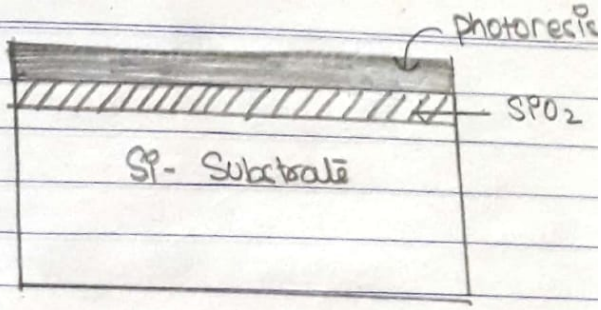
The first step in the process of fabrication involves taking of a substrate of silicon (p-type)



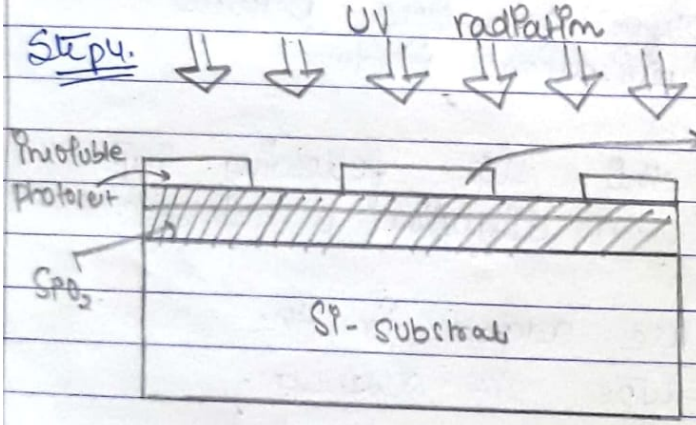
Step 2. It involves adding layer of SiO_2 over the SP substrate



Step 3 In this step we add a layer of photoresist over the layer of SiO_2.

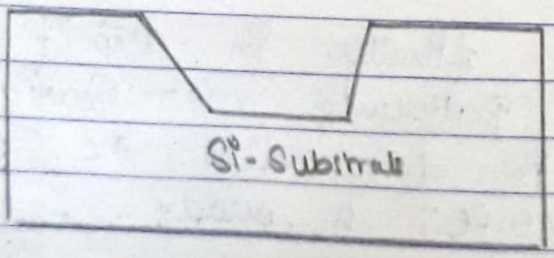


Step 4.



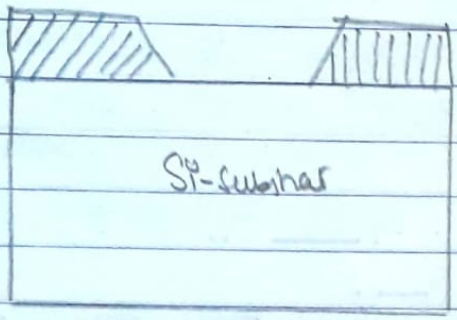
In this step Ultra violet radiations are passed on the substrate for the marking of photoresist. Insoluble and soluble photoresist are present.

Step 5.



In this step photoresist is removed and a window is created.

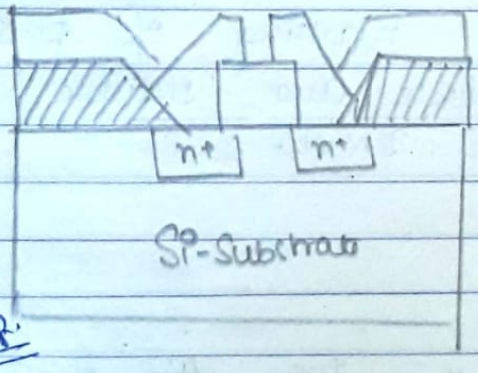
Step 6.



In step (6) the SiO_2 is added again to the window formation on the Si- substrate (p type) i.e here patterned polymerisation is done.

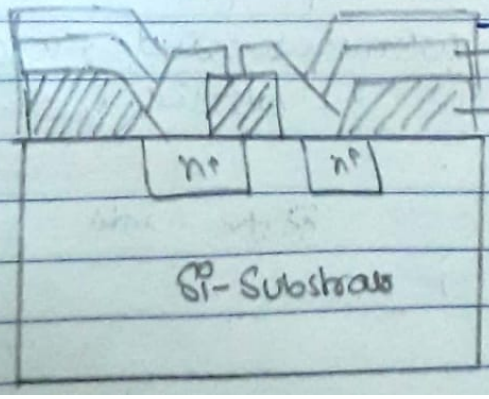
Step 7.

In this step following step (6) n+ diffusion is done.



n+ are added in the p-type Si- substrate.

Step 8.



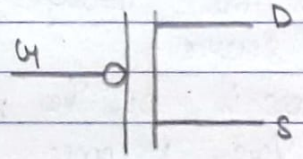
Finally, in step (7) patterned metallization is done and the MOSFET is ready

Hence, fabrication is done.

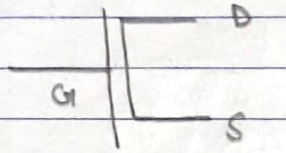
Answer!

(a) MOS transistor → MOS is Metal oxide semiconductor MOS transistor types

(1) P-MOS symbol



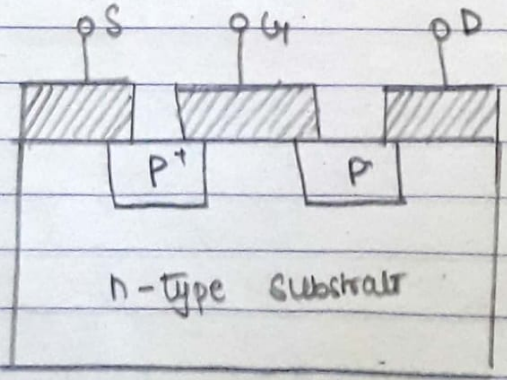
(2) N-MOS symbol



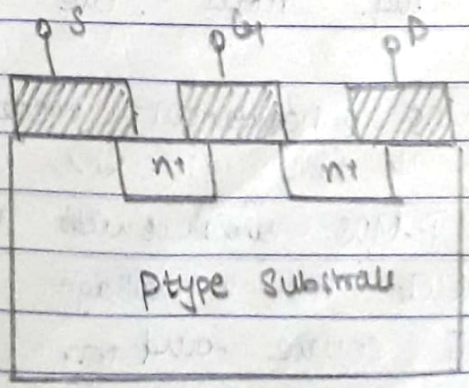
The basic symbol of P-MOS and N-MOS transistor is same almost but to differ the PMOS has a not in it's symbol.

(1) PMOS ckt

~~N-MOS enhancement~~

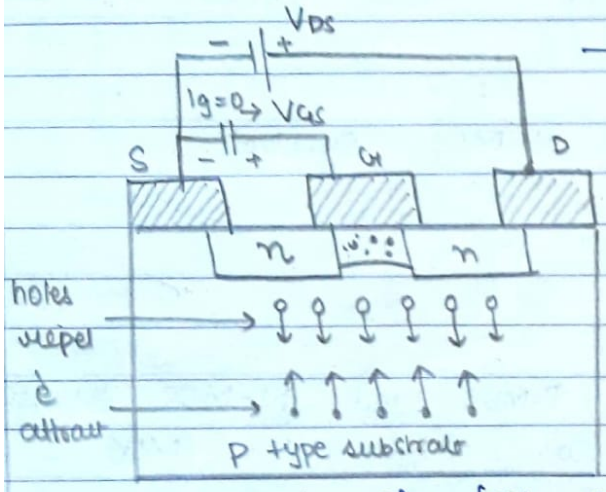


(2) N-MOS ckt.



Here S is Source
D is Drain
G is Gate

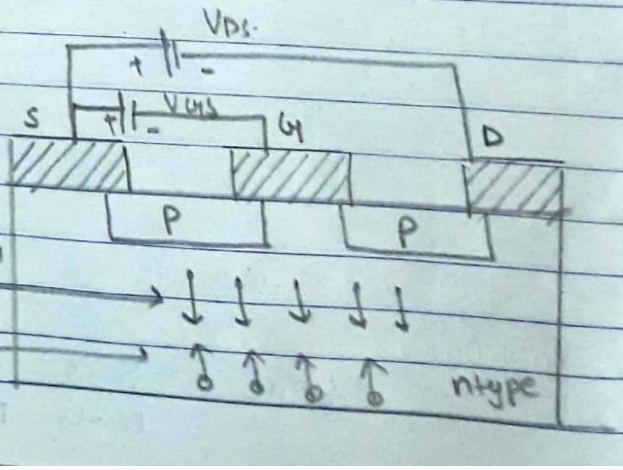
Nmos enhancement mode transistor.



→ from fig VGS is the voltage between source and gate
→ Ig is the Gate current
→ VDS is the voltage between drain and source.
→ When VDS is positive ; the value of VGS becomes zero and no current flows between source and G due to Insulation of Gate and drain to source and also presence of reverse bias P-N function.
→ When VDS is positive & underlying Gate turn from n type to p type as the electrons are attracted and holes are repelled.

P MOS enhancement Mode transistor.

In P-MOS enhancement Mode transistor VDS is voltage between source and drain VGS b/w Gate and source. IG is gate current.

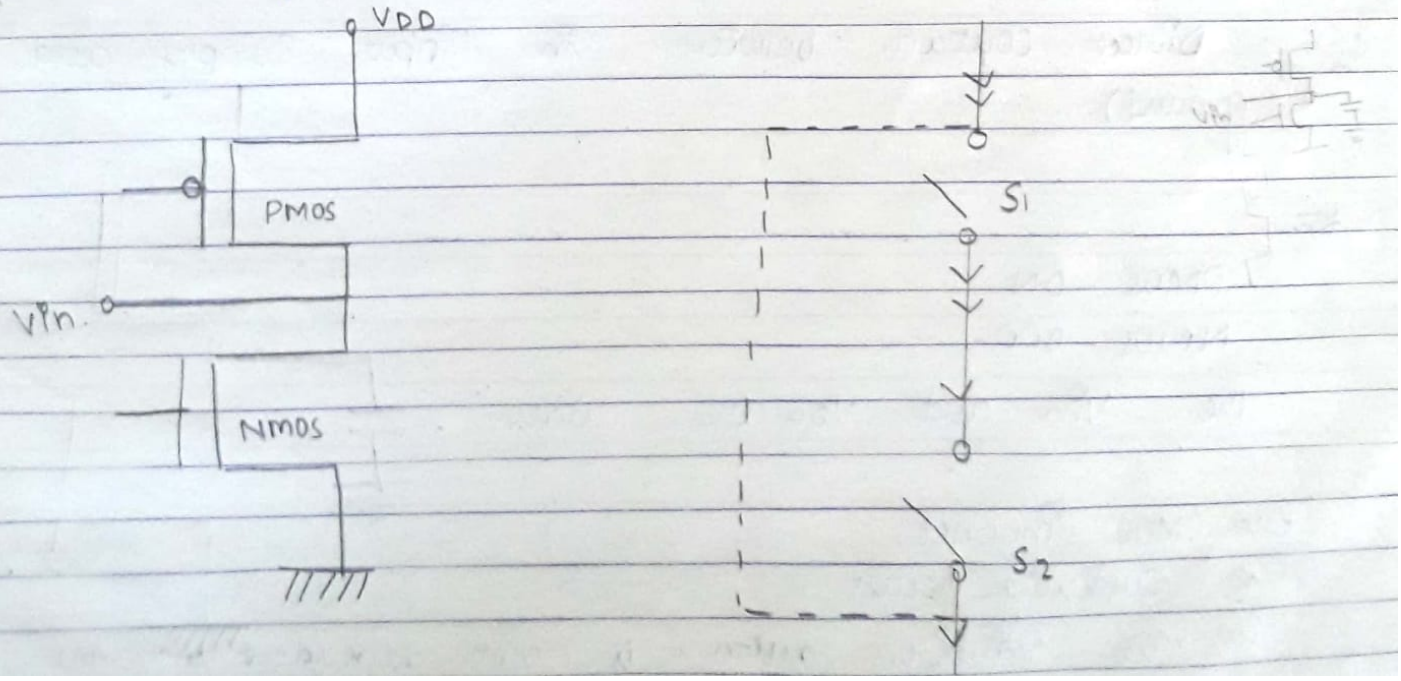


→ When V_{DS} is negative; value of V_{GS} becomes positive and current flow between source and gate due to presence of forward bias P-N junction.

→ When V_{DS} is negative carriers turn from n type to p-type as electrons are repelled and holes are attracted.

Set 2:

CMOS logic Inverter



CMOS Inverter consists of one PMOS and One NMOS transistor which are both connected serially.

There are two modes in which CMOS Inverter acts (1) when PMOS is OFF (2) when NMOS is OFF

*
PMOS - OFF
NMOS - ON
Direct contact between Vin (Input Supply and ground).

*
PMOS - ON
NMOS - OFF
the Vin and VDD are high

In CMOS Inverter
* Switching occurs
* The transistor action is not dependent on the size of transistor so transistor can be of minimum size.
* The noise margin is high.