Estad in year 2000

RIET | RAJASTHAN INSTITUTE OF ENGINEERING & TECHNOLOGY

Approved by AICTE & Affiliated to Rajasthan Technical University

Department of Computer science & Engineering

Time Table 2016-17

VIII semester **w.e.f- 16/01/2017**

	I	II	III	IV	V	Lunch	VI	VII
	8:10-9:05	**9:05-10:00**	**10:00-10:55**	**10:55-11:50**	**11:50-12:45**	**12:45-01:40**	**01:40-2:35**	**02:35-3.30**
Mon.	DIP	MC	UNIX & NETWORKING LAB-3(A4)			LUNCH	RTS	DS
			FPGA LAB-1(A3)					
			INTERNERT FOR PROJECT	DIP LAB-2(A1)				
				PROJECT-II LAB-8(A2)				
Tues.	DS	RTS	FPGA LAB-1(A2)				MC	DIP
			INTERNERT FOR PROJECT	PROJECT-II LAB-8(A1)				
				SEMINAR -(A3)				
				DIP LAB-2(A4)				
Wed.	MC	DIP	UNIX & NETWORKING LAB-8(A2)				RTS	
			FPGA LAB-1(A1)					
			INTERNERT FOR PROJECT	PROJECT-II LAB-8(A3)				
				SEMINAR -(A4)				
Thurs.	RTS	DS	UNIX & NETWORKING LAB-3(A3)				DIP	
			INTERNERT FOR PROJECT	DIP LAB-2(A2)				
				SEMINAR -(A1)				
				PROJECT-II LAB-8(A4)				
Fri.	MC	DS	UNIX & NETWORKING LAB-8(A1)					
			FPGA LAB-1(A4)					
			INTERNERT FOR PROJECT	SEMINAR -(A2)				
				DIP LAB-2(A3)				

SUBJECT : FACULTY NAME

RTS: Dr. SAROJ HIRANWAL
DIP: Mr. VIJAY KUMAR SHARMA
MC: Mr. SUNIL KUMAR
DS: Ms. AKANKSHA

LABS : FACULTY NAME

FPGA: Mr. AMIT BAIRWA
UNIX : Mr. SUNIL KUMAR
PROJECT-II : MS. SHIKHA CHOUDHARY
DIP LAB : Mr. Mr. VIJAY KUMAR SHARMA
SEMINAR : Mr. MUKESH CHOUDHARY