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**Department of Electronics and Communication Engineering**

**Practical Examination & CRT Schedule**

**IV Year (VII SEM)**

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| **S.No.** | **Date** | **Timing** | **Practical Examination & CRT Schedule** |
| 1 | 04/12/2017 | 8:10-10:10 | **Wireless Communication Lab** **(EXTERNAL)**Internal Examiner**:-** Mr. Vivek KhandelwalExternal Examiner:-Ms. Yashika Saini |
| 10:10- 10:30 | BREAK |
| 10:30-1:30 | CRT SESSION -I |
| 1:30- 2:00 | LUNCH |
| 2:00-5:00 | CRT SESSION -II |
| 2 | 05/12/2017 | 8:10-10:10 | **Signal & Image Processing Lab (EXTERNAL)**Internal Examiner**:-** Mr. Snehashis JhaExternal Examiner:- Mr. Gajendra Sujediya |
| 10:10- 10:30 | BREAK |
| 10:30-1:30 | CRT SESSION -I |
| 1:30- 2:00 | LUNCH |
| 2:00-5:00 | CRT SESSION -II |
| 3 | 06/12/2017 | 8:10-10:10 | **Practical Training & Industrial Visit (INTERNAL)**Internal Examiner**:-** Ms. Yashika Saini |
| 10:10- 10:30 | BREAK |
| 10:30-1:30 | CRT SESSION -I |
| 1:30- 2:00 | LUNCH |
| 2:00-5:00 | CRT SESSION -II |
| 4 | 07/12/2017 | 8:10-10:10 | **Project-I (INTERNAL)**Internal Examiner**:-** Mr. Sandeep |
| 10:10- 10:30 | BREAK |
| 10:30-1:30 | CRT SESSION -I |
| 1:30- 2:00 | LUNCH |
| 2:00-5:00 | CRT SESSION -II |

**NOTE: - The schedule of PTS (external) and Project-I (external) will be displayed shortly.**

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**Department of Electronics and Communication Engineering**

**External Examination Schedule**

**III Year (V SEM)**

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| **S.No.** | **Date** | **Lab** | **Internal Examiner** | **External Examiner** | **Timing Slot** |
| 1 | 05/12/2017 | Communication Lab-I | Mr. Nazar Mohammad | Ms. Yashika saini | 9:00-11:00 |
| 2 | 05/12/2017 | Microwave Engg. Lab | Mr. Snehashis Jha | Mr. Shashikaant Ray | 1:00-3:00 |
| 3 | 06/12/2017 | Electronic Eng. Design Lab | Mr. Snehashis Jha | Mr. Vivek Khandelwal | 9:00-11:00 |
| 4 | 06/12/2017 | Signal Processing Lab | Mr. Gajendra Sujediya | Mr. Snehashis Jha | 1:00-3:00 |
| 5 | 07/12/2017 | Professoinal Ethics and Disaster Management | Ms. Priya  | Mrs. Vijaya Chakarwati | 9:00-11:00 |
| 6 | 07/12/2017 | Discipline & Extra Curricular Activity | Mr. Vivek Khandelwal | Mr. Shashikaant Ray | 1:00-3:00 |

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**Department of Electronics and Communication Engineering**

**Internal Examination Schedule**

**III Year (V SEM)**

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| **S.No.** | **Date** | **Lab** | **Internal Examiner** | **Timing Slot** |
| 1 | 04/12/2017 | Electronic Eng. Design Lab | MR. SNEHASHIS JHA | 11:00-1:00 |
| 2 | 04/12/2017 | MICROWAVE ENGG. LAB | MR. SNEHASHIS JHA | 1:30:3:30 |

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