**Rajasthan Institute of Engineering & Technology, Jaipur**

**Department of Computer Engineering**

**B.Tech I MID Term examination**

**Session: 2018-19**

**VII Semester CSE Branch**

**CAD for VLSI Set-A**

Time: 2 hrs. M.M.:20

**Instruction for students:**

1. No provision for supplementary answer book.

Q.1What is Moore’s law? Explain Gajski & Kuhn’s Y-chart with defining the various complexity in microelectronic circuit design.

Or

Q.1 Explain programmable logic devices in detail? Also explain the design flow process of microelectronic circuit with the appropriate diagram.

Q.2 Explain the various levels of abstractions of circuit models?

Or

Q.2 What is Synthesis. Explain all types of Synthesis also.

Q.3 Calculate the Boolean derivative, cofactor, smoothing and consensus of f= ab + bc + ac w.r.t. to a.

Or

Q.3What is ITE Operator? Explain the ITE Algorithm with example.

Q.4 Draw the OBDD and ROBDD of f= x1x2 + x3 for order x1, x2, x3.

Or

Q.4 Explain the distinctive features of Hardware descriptive language. Give an example of Structural hardware modeling.