**Rajasthan Institute of Engineering & Technology, Jaipur**

**Department of Computer Engineering**

**B.Tech I MID Term examination**

**Session: 2018-19**

**VII Semester CSE Branch**

**CAD for VLSI Set-B**

Time: 2 hrs. M.M.:20

**Instruction for students:**

1. No provision for supplementary answer book.

Q.1What is the different semi-custom Design styles for circuits?

Or

Q.1 Explain the four phases in creating microelectronics chips in CAD synthesis and optimization?

Q.2 Explain the various views of circuit models?

Or

Q.2 What is optimization? Explain the optimization techniques for digital circuits.

Q.3 Calculate the Boolean derivative, cofactor, smoothing and consensus of f= (a+b) (b+c) (a+c) w.r.t. to a.

Or

Q.3What is Unique table? Explain the Quantify Algorithm for generating Boolean expressions.

Q.4 Draw the OBDD and ROBDD of f= ab + ac + bc for order (a, b, c).

Or

Q.4 Show how an input a: = b + c\* 60 get processed in compiler. Show the output at each stage of compiler.