**Set- A**

**Rajasthan Institute of Engineering & Technology, Jaipur.**

**I Mid Term examination**

**Session: 2018-19**

**B. Tech. V SEM & Branch: CSE**

**Subject with code: 5CS2A Digital Logic Design**

Time: 2 hrs. M.M.:20

**Instruction for students:**

1. No provision for supplementary answer book.
2. All questions carry equal marks.

Q.1 Write VHDL code for rising edge J-K flip flop by using behavioral modelling.

Or

Q.1 When was the language VHDL standardized and by whom? Give the basic requirements of VHDL.

Q.2 Describe about Sub program using component in detail.

Or

Q.2 Define Data types and discuss its types in brief.

Q.3 Write the VHDL code for XOR gate and draw its appropriate Diagram.

Or

Q.3 Establish comparison between simulation and synthesis in tabular form.

Q.4 Write three differences between package and entity (assume any example).

Or

Q.4 Describe about Look ahead carry adder using appropriate example.

**Set- B**

**Rajasthan Institute of Engineering & Technology, Jaipur.**

**I Mid Term examination**

**Session: 2018-19**

**B. Tech. V Sem & Branch: CSE**

**Subject with code: 5CS2A Digital Logic Design**

Time: 2 hrs. M.M.:20

**Instruction for students:**

1. No provision for supplementary answer book.
2. All questions carry equal marks.

Q.1 Describe concurrent statements using appropriate example.

Or

Q.1 Write short notes on :- (a) Packages (b) Aliases.

Q.2 Write VHDL code for rising edge D flip flop by using behavioral modelling.

Or

Q.2 What do you mean by resolved signals? Explain.

Q.3 What is difference between Simulation and Synthesis?

Or

Q.3 How many type of HDL in world. Give names & use and define following: i) module ii) Modeling iii) Entity.

Q.4 Write are difference between generate and concurrent statement.

Or

Q.4 Write the VHDL code for a half adder circuit using all types of modelling.