Rajasthan Institute of Engineering & Technology, Jaipur.

I Mid Term Examination
Session: 2018-19
5th Semester & Branch EE/EEE
SUBJECT: POWER ELECTRONICS

SET-A

Time: 2 hrs. M.M.:20

Q.1 Define string efficiency and also explain parallel operation of thyristor.

$$String\ efficiency = \frac{V_{oi}\ or\ actual\ current\ rating\ of\ the\ whole\ string}{nos\ of\ SCR\ in\ the\ string\ \times V_{oi}\ or\ current\ rating\ of\ individual\ SCR}$$

Parallel Operation of SCR

When the operating current is more than the individual current ratings of SCRs then we use more than one SCRs in parallel. Due to different V-I characteristics SCRs of same rating shares unequal current in a string. Let a string consists of two transistors in parallel as shown in fig. 1 and their current rating by 1 KA. From the V-I characteristics of the devices it can be seen that for operating volume V, current through SCR_1 is 1 KA and that through SCR_2 is 0.8 KA. Hence, SCR_2 is not fully utilized here. Though the string should withstand R KA theoretically it is only capable of handling 1.8 KA. So, the string efficiency is = 90%. Due to unequal current division when current through SCR increases, its temperature also increases which in turn decreases the resistance. Hence further increase in current takes place and this is a cumulative process. This is known as thermal 'run away' which can damage the device. To overcome this problem SCRs would be maintained at the same temperature. This is possible by mounting them on same heat sink. They should be mounted in symmetrical position as flux. Linkages by the devices will be same. So, the mutual inductance of devices will be same. This will offer same reactance through every device. Thus reducing the difference in current level through the devices. Another way of equalizing the current division in ac circuit can be achieved by using magnetic coupled reactance When $I_1 = I_2$ then resultant flux is zero as two coils are connected in anti-parallel. So, the inductance of the both path will be same. If $I_1 > I_2$ then there will be a resultant flux. This flux induces emfs in cols. 1 and 2 as shown in fig. Hence current in path 1 is opposed and in path 2 it is aided by the induced emfs. Thus reducing the current difference in the paths.

Or

Q.1 In UJT triggering oscillator R= 6.8kohm C=0.1μF.If η =0.82.calculet the frequency of oscillation of relaxation oscillator.

Q.2 Explain switching characteristics of SCR. [5]

Turn ON Time of SCR

A forward biased thyristor can be turned on by applying a positive voltage between gate and cathode terminal. But it takes some transition time to go from forward blocking mode to forward conduction mode. This transition time is called turn on time of SCR and it can be subdivided into three small intervals as delay time (t_d) rise time(t_r), spread time(t_s).

Delay Time of SCR

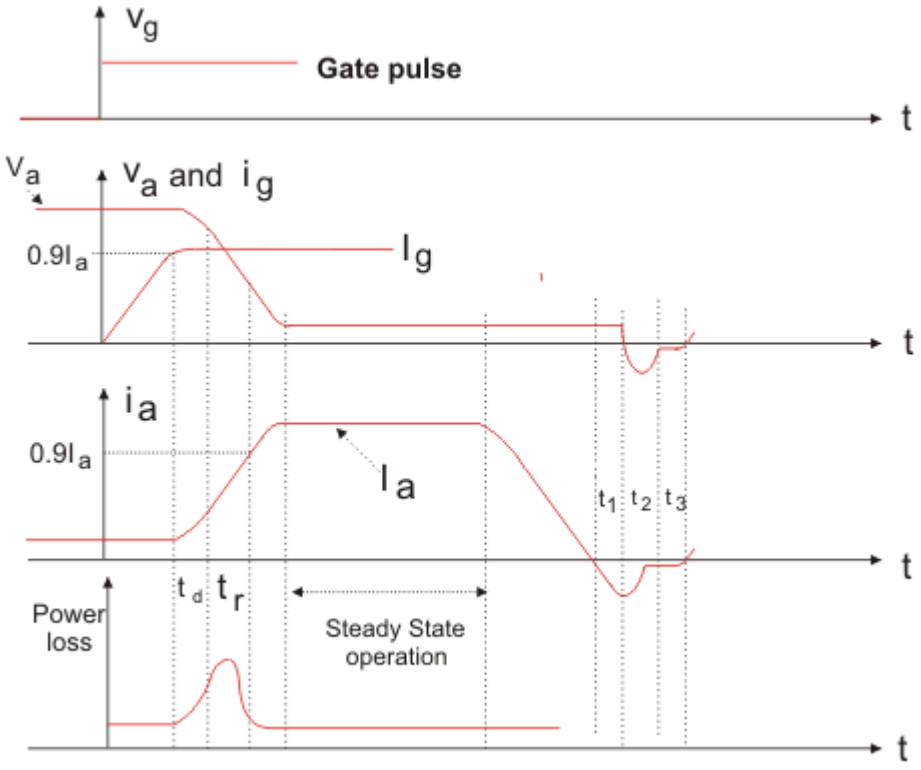
After application of gate current, the thyristor will start conducting over a very tiny region. Delay time of SCR can be defined as the time taken by the gate current to increase from 90% to 100% of its final value I_g. From another point of view, delay time is the interval in which anode current rises from forward leakage current to 10% of its final value and at the same time anode voltage will fall from 100% to 90% of its initial value V_a.

Rise Time of SCR

Rise time of SCR in the time taken by the anode current to rise from 10% to 90% of its final value. At the same time anode voltage will fall from 90% to 10% of its initial value V_a. The phenomenon of decreasing anode voltage and increasing anode current is entirely dependent upon the type of the load. For example if we connect a inductive load, voltage will fall in a faster rate than the current increasing. This is happened because induction does not allow initially high voltage change through it. On the other hand if we connect a capacitive load it does not allow initial high voltage change through it, hence current increasing rate will be faster than the voltage falling rate. High increasing rate of di_a/dt can create local hot spot in the device which is not suitable for proper operation. So, it is advisable to use a inductor in series with the device to tackle high di_a/dt. Usually value of maximum allowable di/dt is in the range of 20 to 200 A per microsecond.

Spread Time of SCR

It is the time taken by the anode current to rise from 90% to 100% of its final value. At the same time the anode voltage decreases from 10% of its initial value to smallest possible value. In this interval of time conduction spreads all over the area of cathode and the SCR will go to fully ON State. Spread time of SCR depends upon the cross-sectional area of cathode.



Turn OFF Time of SCR

Once the thyristor is switched on or in other point of view, the anode current is above latching current, the gate losses control over it. That means gate circuit cannot turn off the device. For turning off the SCR anode current must fall below the holding current. After anode current fall to zero we cannot apply forward voltage across the device due to presence of carrier charges into the four layers. So we must sweep out or recombine these charges to proper turn off of SCR. So turn off time of SCR can be defined as the interval between anode current falls to zero and device regains its forward blocking mode. On the basis of removing carrier charges from the four layers, turn off time of SCR can be divided into two time regions,

1. Reverse Recovery Time.
2. Gate Recovery Time

Reverse Recovery Time

It is the interval in which change carriers remove from J_1, and J_3 junction. At time t_1, anode current falls to zero and it will continue to increase in reverse direction with same slope (di/dt) of the forward decreasing current. This negative current will help to sweep out the carrier charges from junction J_1 and J_3. At the time t_2 carrier charge density is not sufficient to maintain the reverse current hence after t_2 this negative current will start to decrease. The value of current at t_2 is called reverse recovery current. Due to rapid decreasing of anode current, a reverse spike of voltage may appear across the SCR. Total recovery time t_3 - t_1 is called reverse recovery time. After that, device will start to follow the applied reverse voltage and it gains the property to block the forward voltage.

Gate Recovery Time

After sweeping out the carrier charges from junction J_1 and J_3 during reverse recovery time, there still remain trapped charges in J_2 junction which prevent the SCR from blocking the forward voltage. These trapped charge can be removed by recombination only and the interval in which this recombination is done, called gate recovery time.

Or

Q.2 Explain di/dt and dv/dt protection of SCR.

High di/dt Protection

When a thyristor is turned on by gate pulse then charge carriers spread through its junction rapidly. But if rate of rise of anode current, i.e. di/dt is greater than the spreading of charge carriers then localized heat generation will take place which is known as local hot spots. This may damage the thyristor. **Protective Measure :** To avoid local hot spots we use an inductor in series with the device as it prevents high rate of change of current through it.

High dv/dt Protection

When a thyristor is in forward blocking state then only J_2 junction is reverse biased which acts as a capacitor having constant capacitance value C_j (junction capacitance). As we know that current through capacitor follows the relation

$$i = C\frac{dv}{dt} \Rightarrow i \propto \frac{dv}{dt}(if\ C\ constant)$$

Hence leakage current through the J_2 junction which is nothing but the leakage current through the device will increase with the increase in dv_a/dt i.e. rate of change of applied voltage across the thyristor. This current can turn-on the device even when the gate signal is absent. This is called dv/dt triggering and must be avoided which can be achieved by using Snubber circuit in parallel with the device.

Q.3 Explain Gate protection of SCR. [5]

Gate Protection of Thyristor

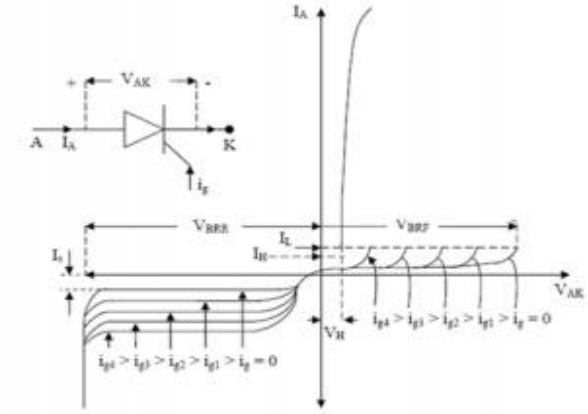
Like thyristor, Gate circuit should also be protected from over voltages and over currents. Over voltages in the gate circuit can cause false triggering and over current can cause high junction temperature. Protective Measure : Over voltages thyristor protection is achieved by using a zener diode and a resistor can be used to protect the gate circuit from over current. Noise in gate circuit can also cause false triggering which can be avoided by using a resistor and a capacitor in parallel. A diode (D) may be connected in series or in parallel with the gate to protect it from high reverse voltage.

Or

Q.3 Explain the working & characteristics of power SCR.

With the help of v-I characteristics we can easily explain the operation SCR, there are three modes of operation. v-I characteristics of SCR is a graph of anode current I A on y-axis &

anode to cathode Voltage plotted on x-axis v-I characteristics can be split into two parts namely Forward Characteristics & Reverse Characteristics
Steady State Characteristics of SCR



There are three modes of operation for an SCR depending upon the biasing given to it:

Forward blocking mode
In this mode of operation the anode is given a positive potential while the cathode is given a negative voltage keeping the gate at zero potential i.e. disconnected. In this case junction J1 and J3 are forward biased while J2 is reversed biased due to which only a small leakage current flows from the anode to the cathode until the applied voltage reaches its breakover value at which J2 undergoes avalanche breakdown and at this breakover voltage it starts conducting but below breakover voltage it offers very high resistance to the flow of current and is said to be in off state.

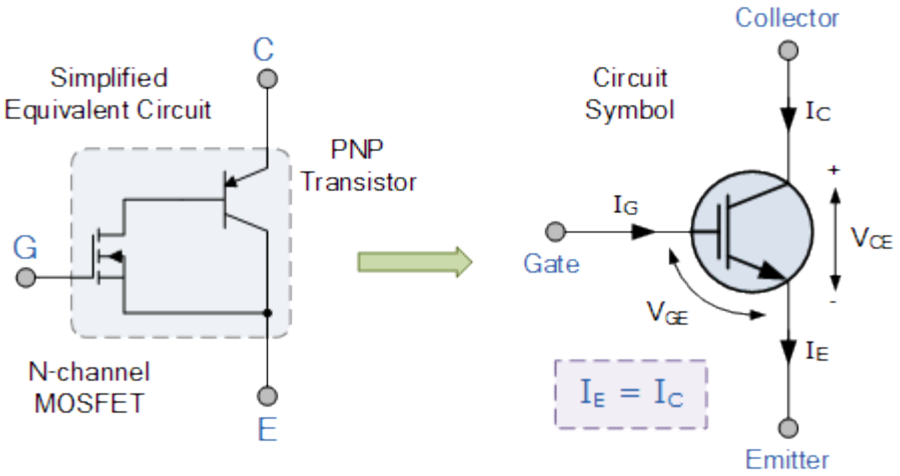
Forward conduction mode
SCR can be brought from blocking mode to conduction mode in two ways – either by increasing the voltage across anode to cathode beyond breakover voltage or by applying of positive pulse at gate. Once it starts conducting no more gate voltage is required to maintain it in on state. There is one way to turn it off i.e. Reduce the current flowing through it below a minimum value called holding current.

Reverse blocking mode
SCR are available with reverse blocking capability. Reverse blocking capability adds to the forward voltage drop because of the need to have a long, low doped P1 region. (If one cannot determine which region is P1, a labeled diagram of layers and junctions can help).
Usually, the reverse blocking voltage rating and forward blocking voltage rating are the same. The typical application for reverse blocking SCR is in current source inverters.

Q.4 What is IGBT? Give its basic structure and working. [5]

The Insulated Gate Bipolar Transistor also called an IGBT for short, is something of a cross between a conventional *Bipolar Junction Transistor*, (BJT) and a *Field Effect Transistor*, (MOSFET) making it ideal as a semiconductor switching device.

The *IGBT Transistor* takes the best parts of these two types of common transistors, the high input impedance and high switching speeds of a MOSFET with the low saturation voltage of a bipolar transistor, and combines them together to produce another type of transistor switching device that is capable of handling large collector-emitter currents with virtually zero gate current drive. Insulated Gate Bipolar Transistor



We can see that the insulated gate bipolar transistor is a three terminal, transconductance device that combines an insulated gate N-channel MOSFET input with a PNP bipolar transistor output connected in a type of Darlington configuration.

As a result the terminals are labelled as: Collector, Emitter and Gate. Two of its terminals (C-E) are associated with the conductance path which passes current, while its third terminal (G) controls the device.

The amount of amplification achieved by the *insulated gate bipolar transistor* is a ratio between its output signal and its input signal. For a conventional bipolar junction transistor, (BJT) the amount of gain is approximately equal to the ratio of the output current to the input current, called Beta.

For a metal oxide semiconductor field effect transistor or MOSFET, there is no input current as the gate is isolated from the main current carrying channel. Therefore, an FET's gain is equal to the ratio of output current change to input voltage change, making it a transconductance device and this is also true of the IGBT. Then we can treat the IGBT as a power BJT whose base current is provided by a MOSFET.

The Insulated Gate Bipolar Transistor can be used in small signal amplifier circuits in much the same way as the BJT or MOSFET type transistors. But as the IGBT combines the low conduction loss of a BJT with the high switching speed of a power MOSFET an optimal solid state switch exists which is ideal for use in power electronics applications.

Also, the IGBT has a much lower "on-state" resistance, R_{ON} than an equivalent MOSFET. This means that the I^2R drop across the bipolar output structure for a given switching current is much lower. The forward blocking operation of the IGBT transistor is identical to a power MOSFET.

When used as static controlled switch, the insulated gate bipolar transistor has voltage and current ratings similar to that of the bipolar transistor. However, the presence of an isolated gate in an IGBT makes it a lot simpler to drive than the BJT as much less drive power is needed.

An insulated gate bipolar transistor is simply turned “ON” or “OFF” by activating and deactivating its Gate terminal. Applying a positive input voltage signal across the Gate and the Emitter will keep the device in its “ON” state, while making the input gate signal zero or slightly negative will cause it to turn “OFF” in much the same way as a bipolar transistor or eMOSFET. Another advantage of the IGBT is that it has a much lower on-state channel resistance than a standard MOSFET.

or

Q.4 Four SCR are to be connected in series. permissible difference in blocking voltage is 20 v for maximum difference in their blocking current of 1ma.difference in recovery charge is 10 µC design equalizing circuit.

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Q.1 Explain various turning on methods of a thyristor. [5]

SCR Triggering or Turn ON Methods

With a voltage applied to the SCR, if the anode is made positive with respect to the cathode, the SCR becomes forward biased. Thus, the SCR comes into the forward blocking state. The SCR can be made to conduct or switching into conduction mode is performed by any one of the following methods.

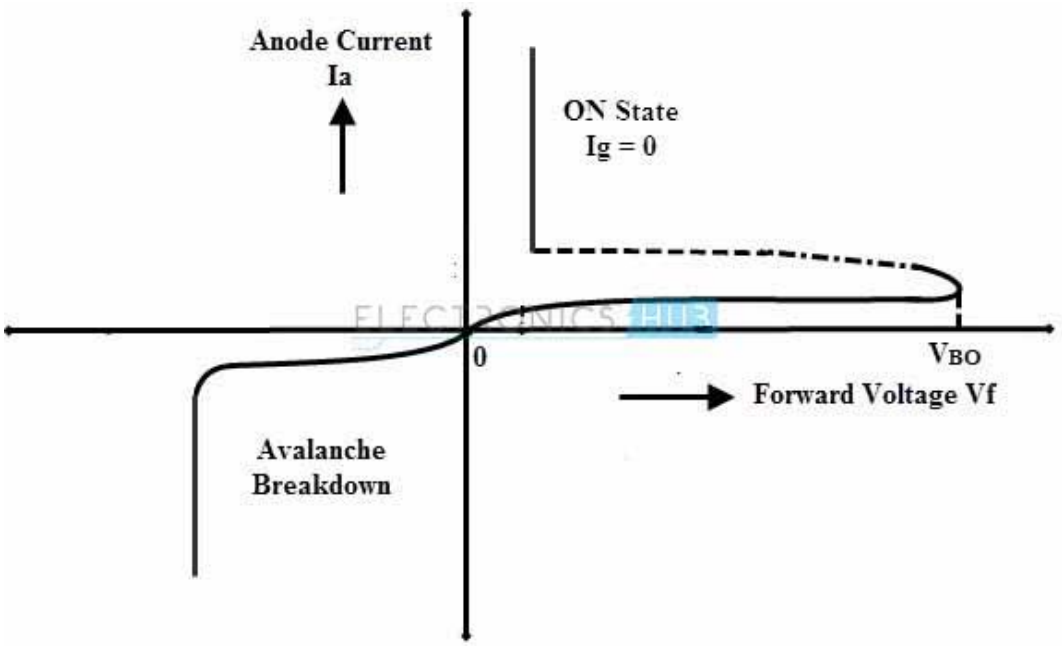
1. Forward voltage triggering
2. Temperature triggering
3. dv/dt triggering
4. Light triggering
5. Gate triggering

1. Forward Voltage Triggering

By increasing the forward anode to cathode voltage, the depletion layer width is also increasing at junction J2. This also causes to increase the minority charge carriers accelerating voltage at junction J2. This further leads to an avalanche breakdown of the junction J2 at a forward breakover voltage VBO.

At this stage SCR turns into conduction mode and hence a large current flow through it with a low voltage drop across it. During the turn ON state the forward voltage drop across the SCR is in the range of 1 to 1.5 volts and this may be increased with the load current.

In practice this method is not employed because it needs a very large anode to cathode voltage. And also once the voltage is more than the VBO, it generates very high currents which may cause damage to the SCR. Therefore, most of the cases this type of triggering is avoided.



2. Temperature Triggering

The reverse leakage current depends on the temperature. If the temperature is increased to a certain value, the number of hole-pairs also increases. This causes to increase the leakage current and further it increases the current gains of the SCR. This starts the regenerative action inside the SCR since the ($\alpha 1 + \alpha 2$) value approaches to unity (as the current gains increases).

By increasing the temperature at junction J2 causes the breakdown of the junction and hence it conducts. This triggering occur in some circumstances particularly when it the device temperature is more (also called false triggering). This type of triggering is practically not employed because it causes the thermal runaway and hence the device or SCR may be damaged.

3. dv/dt Triggering

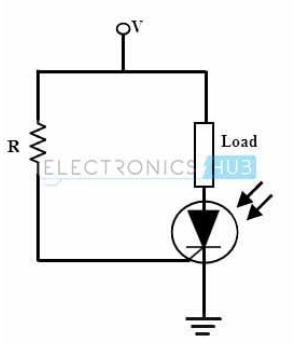
In forward blocking state junctions J1 and J3 are forward biased and J2 is reverse biased. So the junction J2 behaves as a capacitor (of two conducting plates J1 and J3 with a dielectric J2) due to the space charges in the depletion region. The charging current of the capacitor is given as

$$I = C\, dv/ dt$$

where dv/dt is the rate of change of applied voltage and C is the junction capacitance. From the above equation, if the rate of change of the applied voltage is large that leads to increase the charging current which is enough to increase the value of alpha. So the SCR becomes turned ON without a gate signal. However, this method is also practically avoided because it is a false turn ON process and also this can produce very high voltage spikes across the SCR so there will be considerable damage to it.

4. Light Triggering

An SCR turned ON by light radiation is also called as Light Activated SCR (LASCR). This type of triggering is employed for phase controlled converters in HVDC transmission systems. In this method, light rays with appropriate wavelength and intensity are allowed to strike the junction J2.These types of SCRs are consisting a niche in the inner p-layer. Therefore, when the light struck on this niche, electron-hole pairs are generated at the junction J2 which provides additional charge carriers at the junction leads to turn ON the SCR.



5.Gate Triggering

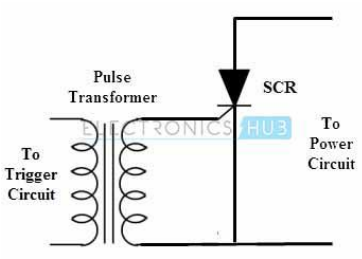
This is most common and efficient method to turn ON the SCR. When the SCR is forward biased, a sufficient voltage at the gate terminal injects some electrons into the junction J2. This result to increase reverse leakage current and hence the breakdown of junction J2 even at the voltage lower than the VBO.Depends on the size of the SCR the gate current varies from a few milli-amps to 200 milli amps or more. If the gate current applied is more, then more electrons are injected into the junction J2 and results to come into the conduction state at much lower applied voltage.In gate triggering method, a positive voltage applied between the gate and the cathode terminals. We can use three types of gate signals to turn On the SCR. Those are DC signal, AC signal and pulse signal.

DC Gate Triggering

In this triggering, a sufficient DC voltage is applied between the gate and cathode terminals in such a way that the gate is made positive with respect to the cathode. The gate current drives the SCR into conduction mode. In this, a continuous gate signal is applied at the gate and hence causes the internal power dissipation (or more power loss).

AC Triggering

This is the most commonly used method for AC applications where the SCR is employed for such applications as a switching device. With the proper isolation between the power and control circuit, the SCR is triggered by the phase-shift AC voltage derived from the main supply. The firing angle is controlled by changing the phase angle of the gate signal.



However, only one half of the cycle is available for the gate drive to control the firing angle and next half of the cycle a reverse voltage is applied between the gate and cathode. This is one of the limitation of AC triggering and also separate step down or pulse transformer is needed to supply the voltage to gate drive from the main supply.

Pulse Triggering

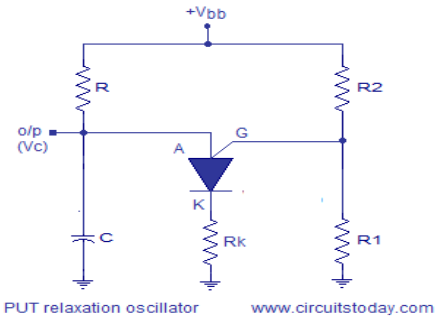
The most popular method of triggering the SCR is the pulse triggering. In this method, gate is supplied with single pulse or a train of pulses. The main advantage of this method is that gate drive is discontinuous or doesn't need continuous pulses to turn the SCR and hence gate losses are reduced in greater amount by applying single or periodically appearing pulses. For isolating the gate drive from the main supply, a pulse transformer is used.

Or

Q.1 **For an SCR the Gate cathode characteristics has a straight line slop of 130.for trigger source voltage of 15v and allowable gate power dissipation of 0.5watts.find gate source resistance.**

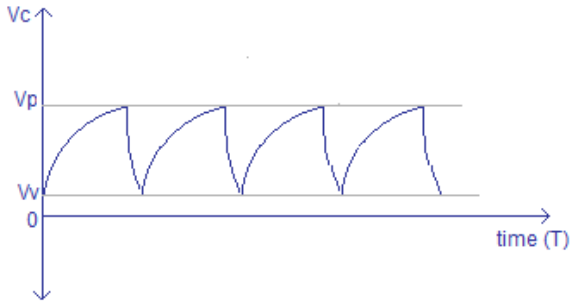
Q.2 Explain the construction & working of relaxation oscillator. give necessary diagrams. **[5]**

Relaxation oscillator is of course the most common application of a programmable UJT. PUT relaxation oscillator can be used for generating a wide range of saw tooth wave forms. It is called a relaxation oscillator because the timing interval is started by the gradual charging of a capacitor and the timing interval is terminated by the sudden discharge of the same capacitor. The circuit diagram of a PUT relaxation oscillator is shown below.



Resistors R1 and R2 set the peak voltage (Vp) and intrinsic standoff ratio (η) of the PUT. Resistor Rk limits cathode current of the PUT. Resistor R and capacitor C sets the frequency

of the oscillator. When the supply voltage Vbb is applied, the capacitor C starts charging through resistor R. When the voltage across the capacitor exceeds the peak voltage (Vp) the PUT goes into negative resistance mode and this creates a low resistance path from anode(A) to cathode(K). The capacitor discharges through this path. When the voltage across the capacitor is below valley point voltage (Vv) the PUT reverts to its initial condition and there will be no more discharge path for the capacitor. The capacitor starts to charge again and the cycle is repeated. This series of charging and discharging results in a sawtooth waveform across the capacitor as shown in the figure below.



Wave form across the capacitor in a PUTrelaxation oscillator

The frequency of oscillation of a PUT relaxation oscillator can be expressed by the following equation:

F = 1/ (RC ln(1/(1-η)).Where F is the frequency, η is the intrinsic standoff ratio, R is the resistance and C is the capacitance.

Or

Q.2 Define string efficiency and Explain series operation of thyristor.

$$String\ efficiency = \frac{V_{oi}\ or\ actual\ current\ rating\ of\ the\ whole\ string}{nos\ of\ SCR\ in\ the\ string\ \times V_{oi}\ or\ current\ rating\ of\ individual\ SCR}$$

Series Operation of SCR

When the operating voltage is more than the rating of one SCR the multiple SCRs of same ratings are used in series. As we know SCR's having same rating, may have different I-V characteristic, so unequal voltage division is bound to take place. For example if two SCRs in series that is capable of blocking 5 KV individually, then the string should block 10 KV. But practically this does not happen. This can be verified with the help of an example.

So we can see from the diagram, for same leakage current, unequal voltage division takes place. Voltage across SCR_1 is V_1 but that across SCR_2 is V_2. V_2 is much less than V_1. So, SCR_2 is not fully utilized. Hence the string can block $V_1 + V_2 = 8$ KV, rather than 10 KV and the string efficiency is given by = 80%. To improve the efficiency a resistor in parallel with every SCR is used. The value of these resistances are such that the equivalent resistance of each SCR and resistor pair will be same. Hence this will ensure equal voltage division across

each SCR. But in practical different rating of resistor is very difficult to use. So we chose one value of

$$R = \frac{nV_{bm} - V_s}{(n-1)\Delta I_b}$$

resistance to get optimum result which is given by
Where, n = no. of SCR in the string V_{bm} = Voltage blocked by the SCR having minimum leakage current. ΔI_b = Difference between maximum and minimum leakage current flowing through SCRs. V_s = Voltage across the string. This resistance b is called static equalizing circuit. But this resistance is not enough to equalize the voltage division during turn on and turn off. In these transient conditions, to maintain the equal volume across each device a capacitor is used along with resistor in parallel with every SCR. This is nothing but snubber ckt which also known as dynamic equalizing circuit. An additional diodes can also be used to improve the performance of dynamic equalizing circuit.

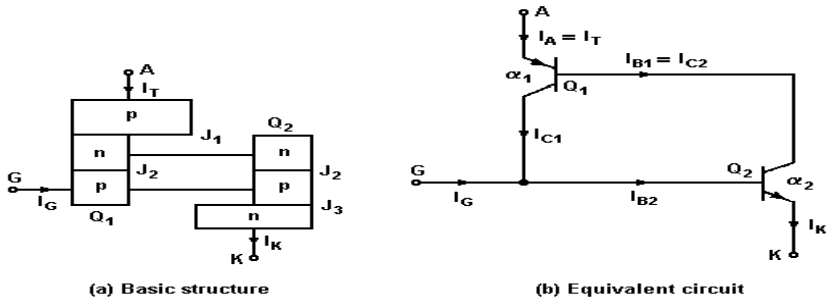
Q.3 **Discuss SCR protection against over voltage current.** **[5]**

Over current mainly occurs due to different types of faults in the circuit. Due to over current i^2R loss will increase and high generation of heat may take place that can exceed the permissible limit and burn the device. Protective Measure : SCR can be protected from over current by using CB and fast acting current limiting fuses (FACLF). CB are used for protection of thyristor against continuous overloads or against surge currents of long duration as a CB has long tripping time. But fast-acting fuses is used for protecting SCR against high surge current of very short duration.

Or

Q.3 Discuss two transistor model of a thyristor.

This model is used to demonstrate the regenerative or latching action due to positive feedback in the thyristor. A thyristor can be considered as two complementary transistors. One being pnp and the other npn. The two transistor model is shown in figure



(a) Basic structure (b) Equivalent circuit

The collector current I_C of a transistor is related to the emitter current I_E and the leakage current of the collector base junction I_{CBO} as

$$I_C = \alpha I_E + I_{CBO} \quad \text{.....(1)}$$

The emitter current of transistor Q_1 is the anode current I_A of the thyristor and collector current I_{C1} is given by

$$I_{C1} = \alpha_1 I_A + I_{CBO1} \quad \text{.....(2)}$$

where a_1 and I_{CBO1} are the current gain and leakage current respectively for transistor Q_1.

Similarly, the collector current for transistor Q_2 is I_{C2} where

$$I_{C2} = \alpha_2 I_k + I_{CBO2} \quad \text{.....(3)}$$

where a_2 and I_{CBO2} are the current gain and leakage current respectively for transistor Q_2.

Combining the two collector currents I_{C1} and I_{C2} yields

$$I_A = I_{C1} + I_{C2}$$

$$I_A = \alpha_1 I_A + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \quad \text{.....(4)}$$

When a gate current I_G is applied to the thyristor

$$I_k = I_A + I_G \quad \text{.....(5)}$$

Solving for anode current I_A in equation 5 yields

$$I_A = \frac{\alpha_2 I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)} \quad \text{.....(6)}$$

The current gain a_1 varies with emitter current I_{E1} which is equal to I_A; and a_2 varies with emitter current I_{E2} which is equal to I_k.

A typical variation of current gain a with emitter current I_E is shown in figure 4.4.

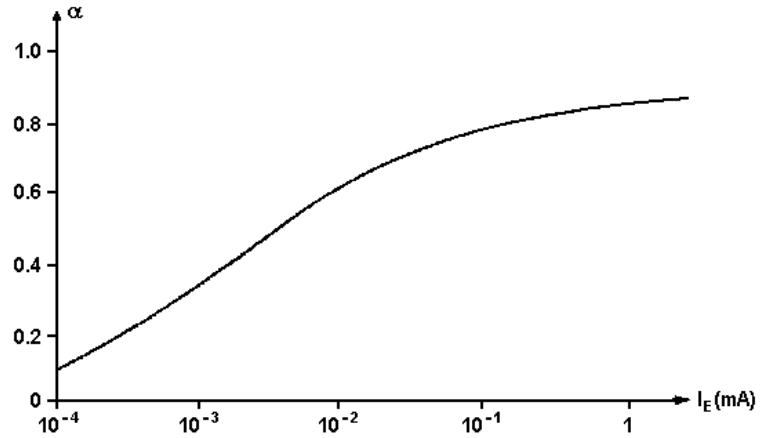


Figure 4.4 Typical Variation of Current Gain With Emitter Current

If the gate current I_G is increased from zero to some positive value, this will increase the anode current I_A as shown by equation 6. An increase of I_A which is an increase of I_{E1} would

increase a_1 as shown in figure 4.4 and also a_2 since $I_{E2} = I_k = I_A + I_G$. The increase in values of both a_1 and a_2 would further increase the value of anode current I_A which is a *regenerative* or *positive feedback effect*.

If a_1 and a_2 approach unity, the denominator of equation 6 approaches zero and a large value of anode current is produced causing the thyristor to turn on as a result of the application of a small gate current.The capacitance of the pn junctions are shown in figure 4.5 below.

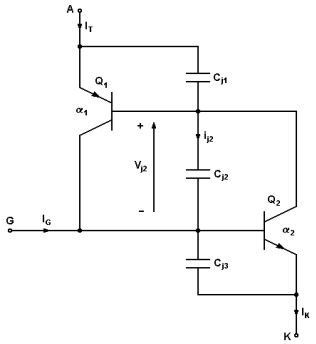


Figure 4.5 Two-transistor Transient Model of Thyristor

Under transient conditions, the capacitances of the pn junctions influence the characteristics of the thyristor.

If a thyristor is in the blocking state and a rapidly rising voltage is applied to the device, high currents would flow through the junction capacitors. The current through capacitor C_{j2} can be expressed as

$$i_{j2} = \frac{d(q_{j2})}{dt} = \frac{d(C_{j2}V_{j2})}{dt} = V_{j2}\frac{dC_{j2}}{dt} + C_{j2}\frac{dV_{j2}}{dt}$$

where

C_{j2} = capacitance of junction j2

V_{j2} = voltage of junction j2

q_{j2} = charge in junction j2

If the rate of rise of voltage dv/dt is large, then i_{j2} would be large, which would result in increased leakage currents I_{CBO1} and I_{CBO2}. High enough values of I_{CBO1} and I_{CBO2} may cause a_1 and a_2 to approach unity, resulting in undesirable turn on of the thyristor.

Q.4 Compare characteristics of MOSFET & IGBT. [5]

MOSFETs:

• Improved switching speeds.

• Improved dynamic performance that requires even less power from the driver.

• Lower gate-to-drain feedback capacitance

• Lower thermal impedance which, in turn, has enabled much better power dissipation

• Lower rise and fall times, which has allowed for operation at higher switching frequencies

IGBTs:

• Improved production techniques, which has resulted in a lower cost

• Improved durability to overloads

• Improved parallel current sharing

• Faster and smoother turn-on/-off waveforms

• Lower on-state and switching losses

• Lower thermal impedance

• Lower input capacitance

Conclusion

MOSFETs and IGBTs are fast replacing a large majority of older solid-state and mechanical devices. It's a movement that doesn't look like it's going to slow down any time soon either, especially with the development of silicon carbide (SiC) material quality. SiC power devices are showing developers advantages like less loss, smaller size, and improved efficiency. Innovations like this will continue to push the limits of MOSFETs and IGBTs into higher-voltage and higher-power applications. As a result, tradeoffs and overlaps are likely to continue in many applications. With that being the case, careful analysis of the device itself is perhaps the most logical solution when faced with the task of selecting a transistor for your SMPS application.

or

Q.4 Four SCR are to be connected in series. Permissible difference in blocking voltage is 20 v for maximum difference in their blocking current of 1ma.difference in recovery charge is 10 µC design equalizing circuit.