CS302-MIDTERM SOLVED SUBJECTIVE WITH REFERENCES

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Q-21

Draw function table of a half adder circuit? (2)

Answer: - Page 135   Lec14

Half-Adder Logic Circuit
         The Half-Adder Logic Circuit can be directly implemented from the Sum and Carry Out Boolean expressions. Figure 14.6
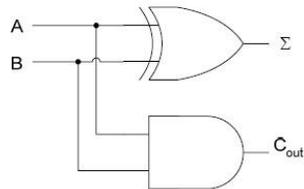

Figure 14.6   Half-Adder Logic Circuit

Q-22

What is difference b/w BCD to decimal decoder and binary 4-to-16 bit decoder? (2)

Answer: (Page 163)   Lec17

The operation of the BCD-to-Decimal Decoder is the same as a Binary 4-to-16 decoder, the only difference being that the BCD-to-Decimal Decoder has ten output pins instead of sixteen and the input is a valid BCD number.

Q-23

Explain major use of decoder circuits? (3)   Lec16

Answer: (Page 158)

Decoders have two major uses in Computer Systems.

1. Selection of Peripheral Devices

Computers have different internal and external devices like the Hard Disk, CD Drive, Modem, Printer etc. Each of these different devices is selected by specifying different codes. A decoder similar to the Electronic Door Lock/Unlock circuit is used to uniquely select or deselect the appropriate devices.

2. Instruction Decoder

Computer programs are based on instructions which are decode by the Computer Hardware and implemented. These instruction codes are decoded by an Instruction Decoder to generate signals that control different logic circuits like the ALU and memory to perform these operations.

Q-25

PALS comes in different configurations and are identified by a unique number, identify parts of this number? (5)

Answer: (Page 186)   Lec19

PALs come in different configurations they are identified by unique number. The numbers begin with the prefix PAL followed by two digits that indicate the number of inputs followed by a letter L active-low, H active-high or P programmable polarity followed by a single or two digits that indicate the number of outputs. In addition to the standard number there may be suffixes which specify the speed, package type and temperature range

Q-26

One of the ABEL entry methods uses logic equation. Explain at least two examples? (5)

Answer: (Page 201)   Lec20

ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'. All ABEL equations must end with ';'.

Examples:-

(a) $X = A\bar{B}C + \overline{ABC} + AB + \bar{B}C$

(b) $Y = (\bar{A} + B + \bar{C} + D)(A + B + C)$

Solution

(a) X = A& !B & C # !A & !B & !C # A & B # !B & C;

(b) Y = (!A # B # !C #D) & (A # B # C);

MIDTERM EXAMINATION 2011 (October-November)

Q-21

Draw the function table of 2-to-4 decoder (2 marks)

Answer: (Page 158)   Lec16

A 2-to-4 Decoder is represented by the function table.

Input		Output			
I_1	I_0	O_0	O_1	O_2	O_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Function Table of a 2-to-4 Binary Decoder

Q-24

**Explain BCD to Decimal Decoder (3marks)**
Answer: (Page 163)   Lec17

"The operation of the BCD-to-Decimal Decoder is the same as a Binary 4-to-16 decoder, the only difference being that the BCD-to-Decimal Decoder has ten output pins instead of sixteen and the input is a valid BCD number. Thus invalid BCD codes 1010, 1011, 1100, 1101, 1110 and 1111 applied at the input of the Decoder do not activate any of the ten outputs."

Q-26

Explain 8-input Multiplexer with the help of circuit Diagram and Function Table. (5marks)
Answer: (Page 170) Lec18

Figure 18.2   8-to-1 Multiplexer using two 4-to-1 Multiplexers
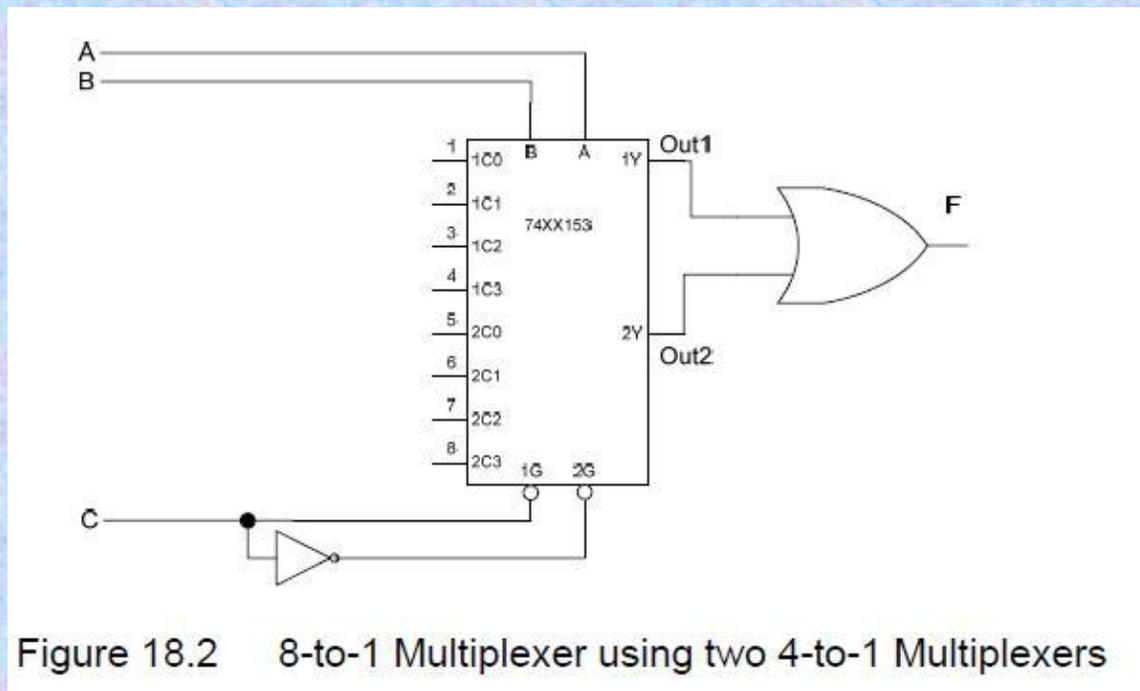
Input			Output
C	B	A	F
0	0	0	1C0
0	0	1	1C1
0	1	0	1C2
0	1	1	1C3
1	0	0	2C0
1	0	1	2C1
1	1	0	2C2
1	1	1	2C3

Q-21

What is meant by ABEL? (2 marks)

Answer: (Page 201) Lec20

ABEL which is an acronym for Advanced Boolean Expression Language is hardware description language used for implementing logic designs using PLDs.

Q-22

Why preferable to use another method than 5-variable K-Map? (2 marks)

Answer: (Page 102) Lec11

Karnuagh map method becomes difficult to manage when numbers of variables exceed 4. In both the Karnaugh maps, finding the redundant terms is not very obvious. The Quine-McCluskey approach of simplifying Boolean expression is based on an exhaustive search where each minterm is compared with every other minterm in order to remove single variables.

Q-24

Draw circuit diagram of 2-input of 8-bit multiplexer? (3 marks)
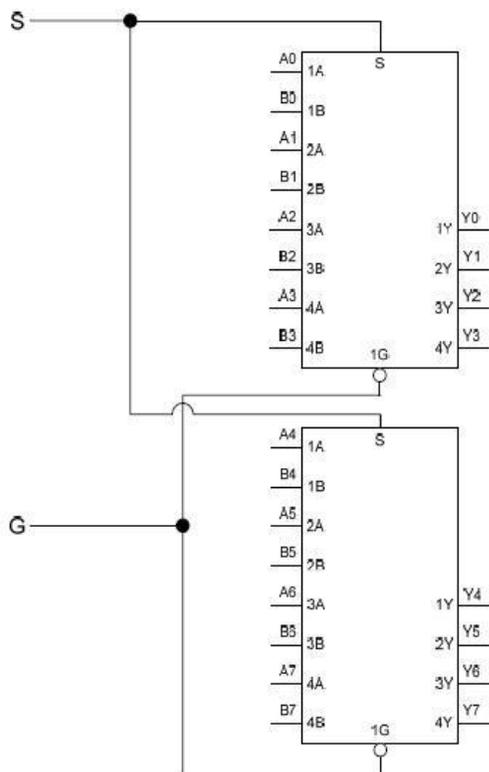
Answer: (Page 172) Lec18

Figure 18.4   2-Input, 8-bit Multiplexer

Q-25
Uses of Demultiplexer?   (5 marks)
Answer: (Page 178)   Lec19
Demultiplexer is used to connect a single source to multiple destinations. One use of the Demultiplexer is at the output of the ALU circuit. The output of the ALU has to be stored in one of the multiple registers or storage units. The Data input of the Demultiplexer is connected to the output of the ALU. Each output of the Demultiplexer is connected to each of the multiple registers. By selecting the appropriate output data from the ALU is routed to the appropriate register for storage.

The second use of the Demultiplexer is the reconstruction of Parallel Data from the incoming serial data stream. Serial data arrives at the Data input of the Demultiplexer at fixed time intervals. A counter attached to the Select inputs of the Demultiplexer routes the incoming serial bits to successive outputs where each bit is stored. When all the bits have been stored, data can be read out in parallel.

MIDTERM EXAMINATION 2011 (October-November)

Q-21
Define Sequential Circuit.   MARKS: 2
Answer: (Page 8) Lec1
Digital circuits that generate a new output on the basis of some previously stored information and the new input are known as Sequential circuits.

Digital circuits that use memory elements for their operation are known as Sequential circuits. **(Page 218)**

Q-22
How a circuit with multiple outputs is shown in truth table?   MARKS: 2
Answer: (Page 103)   Lec11
Circuits having multiple outputs are represented by multiple function tables one for each output or a single function table having multiple output columns. The example of a BCD to 7-Segment Decoder circuit which has 4 inputs and 7 outputs is considered to explain functions having multiple outputs.

Q-23
How decoder is used as demultiplexer.   MARKS: 3:
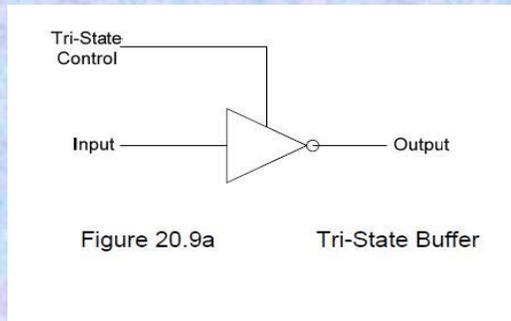**Answer: (Page 178)   Lec19**
A Demultiplexer is available as a Decoder/Demultiplexer chip which can be configured to operate as a Demultiplexer or a Decoder.

Q-21

Draw the Tri_state buffer. 2
Answer: (Page 196)   Lec20

Figure 20.9a   Tri-State Buffer

Q-22

Draw the half adder graph. 2
Answer: (Page 134)   Lec14

Half-Adder
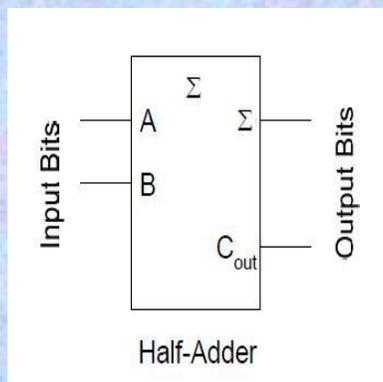
Q-23

Draw NOR gate based S_R (set rest) Latch. 3
Answer: (Page 220)   Lec22

Figure 22.4   NOR based S-R Latch

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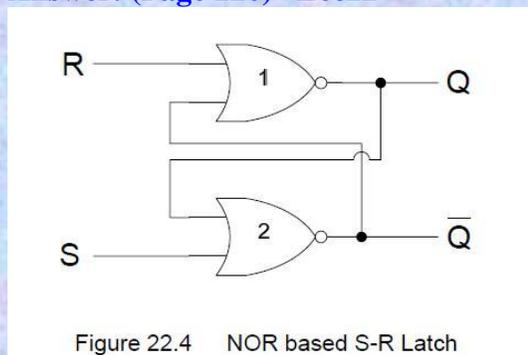
Q-22

Two bit comparator? Explain by at least one example

Answer: (Page 109)   Lec12

A 2-bit Comparator circuit compares two 2-bit numbers A and B. The comparator circuit
has three outputs. It sets the A>B output to 1 if A>B. It sets the A=B output to 1 if A=B and sets A<B output to 1 if A <
B.

Q-23

Explain PLDs

Answer: (Page 179)   Lec19

Programmable Logic Devices are used in many applications to replace the Logic gates and MSI chips. PLDs
save circuit space and reduce and save the cost of components in a Digital Circuit. PLDS consists of Arrays of
AND gates and OR gates that can be programmed to perform specific functions.

Q-24

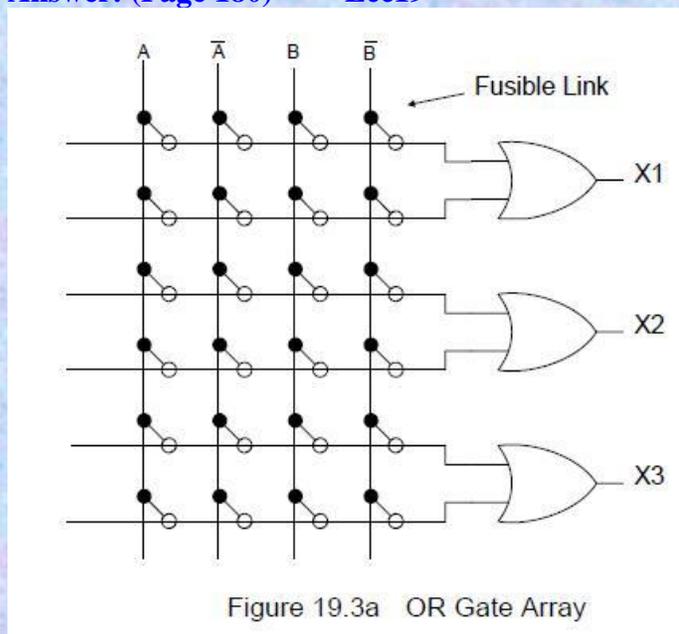**Comparator All possibilities for A = B.**

Answer: (Page 109)   Lec12

• The output A=B is set to 1 when the input combinations are 00 00, 01 01, 10 10 and 11 11

Q-25

one diagram for PLD array with its fuses connecting columns to rows

Answer: (Page 180)   Lec19

Figure 19.3a   OR Gate Array

MIDTERM EXAMINATION 2011(May)

Define decoder   2 marks

Answer:- (Page 157)

A Decoder has multiple inputs and multiple outputs. The Decoder device accepts as an input a multi-bit code and activates one or more of its outputs to indicate the presence of the multi-bit code.

Why S and R input of NAND based latch should not be at logic high at same time   2 marks

Answer:- (Page 220)

When inputs are S = 1 and R = 0 the output Q is set to 0. Inputs S = 0 and R = 0 are not applied as they place the latch in an invalid state. The NAND gate based S-R latch has active-low inputs."

2 input 4 bit multiplexer function table   3 marks

Answer:- (Page 169)

Inputs		Outputs			
G	S	1Y	2Y	3Y	4Y
1	X	0	0	0	0
0	0	1A	2A	3A	4A
0	1	1B	2B	3B	4B

Table 18.1   Function table of 2-Input 4-Bit Multiplexer

Half adder explanation its function table Boolean expression and circuit diagram   5 marks

Answer:- (Page 134)

Half-Adder

A Half-Adder can be fully described in terms of its Function table, its Sum and Carry Out Boolean Expressions and the circuit Implementation.

Half-Adder Function Table

The Half-Adder has a 2-bit input and a 2-bit output. The function table of the Half-Adder has two input columns representing the two single bit numbers A and B. The function table also has two output columns representing the Sum bit and Carry Out bit.

Half-Adder Sum & Carry Out Boolean Expressions

The Sum and Carry Out expressions of the Half-Adder can be determined from the function table. The Half-Adder Sum and Carry Out outputs are defined by the expressions

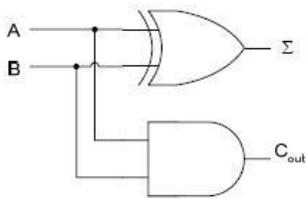$$Sum = \overline{A}B + A\overline{B} = A \oplus B$$
$$CarryOut = AB$$

Figure 14.6   Half-Adder Logic Circuit

Explain S-R latch in your own words

A latch is a temporary storage device that has two stable states. A latch output can change from one state to the other by applying appropriate inputs. A latch normally has two inputs, the binary input combinations at the latch input allows the latch to change its state. A latch has two outputs Q and its complement $\overline{Q}$ The latch is said to be in logic high state when Q=1 and $\overline{Q}$=0 and it is in the logic low state when Q=0 and $\overline{Q}$=1. When the latch is set to a certain state it retains its state unless the inputs are changed to set the latch to a new state. Thus a latch is a memory element which is able to retain the information stored in it.

MIDTERM EXAMINATION 2011

Write down the ABEL symbols that are used for NOT, AND, OR and XOR operations.

NOT=!
AND= &
OR = #
XOR =$.

MIDTERM EXAMINATION 2010

Question No: 17   (Marks: 2)
Why a 2-bit comparator is called parallel comparator?

The 2-bit Comparator discussed earlier is considered to be a Parallel Comparator as all the bits are compared simultaneously. External Logic has to be used to Cascade together two such Comparators to form a 4-bit Comparator.

Question No: 18   (Marks: 2)
Explain at least two advantages of the circuit having low power consumption

Advantages of low power consumption are circuits that can be run from batteries instead of mains power supplies. Thus portable devices that run on batteries.

Secondly, low power consumption means less heat is dissipated by the logic devices; this means that logic gates can be tightly packed to reduce the circuit size without having to worry about dissipating the access heat generated by the logic devices.

Question No: 19   (Marks: 2)
Name the four OLMC configurations
Answer:- (Page 196)
The four OLMC configurations are
   ❖ Combination Mode with active-low output
   ❖ Combinational Mode with active-high output
   ❖ Registered Mode with active-low output
   ❖ Registered Mode with active-high output

Question No: 20   (Marks: 3)
Explain "Test Vector" in context of ABEL
Answer:- (Page 204)
Once the Logic circuit design has been entered its operation is verified by using 'test vectors'. A 'test vector' specifies the inputs and the corresponding outputs. The software simulates the operation of the logic circuit by applying the test vector and checking the outputs. Test vectors are essentially the same as Truth Tables

Question No: 21   (Marks: 3)
For a two bit comparator circuit specify the inputs for which the output A < B is set to 1
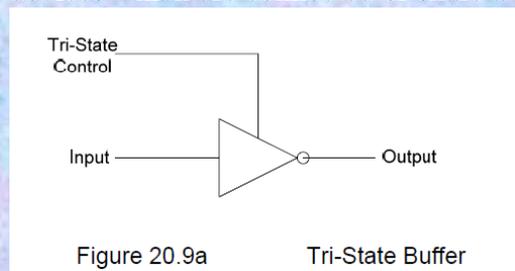**Answer:- (Page 109)**
The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11

Question No: 22   (Marks: 5)
Explain Tri-State Buffers with the help of block diagram
Answer:- (Page 196)
Tri-State Buffer is a NOT gate with a control line that disconnects the output from the input. When the control line is high the buffer operates like a NOT gate and when the control line is low the output is disconnected from the output and high impedance is seen at the output. Tri-state buffers are used to disconnect the outputs of devices which are connected or share a common output line.

Tri-State
Control

Input ————▷○———— Output

Figure 20.9a   Tri-State Buffer

Question No: 23 (Marks: 5)
Explain the Operation of Odd-Parity Generator Circuit with the help of timing diagram
**Answer:- (Page 196)**

The timing diagram shows the operation of the Odd-Parity generator circuit.
The A, B, C and D timing diagrams represent the changing 4-bit data values. During time interval t0 the 4-bit data value is 0000, during time interval t1, the data value changes to 0001.
Similarly during time intervals t2, t3, t4 up to t8 the data values change to 0010, 0011, 0100 and 1000 respectively. During interval t0 the output of the two XOR gates is 0 and 0, therefore the output of the XNOR gate is 1. At interval t1, the outputs of the two XOR gates is 1 and 0, therefore the output of the XNOR gate is 0. The output P can similarly be traced for intervals t2 to t8.
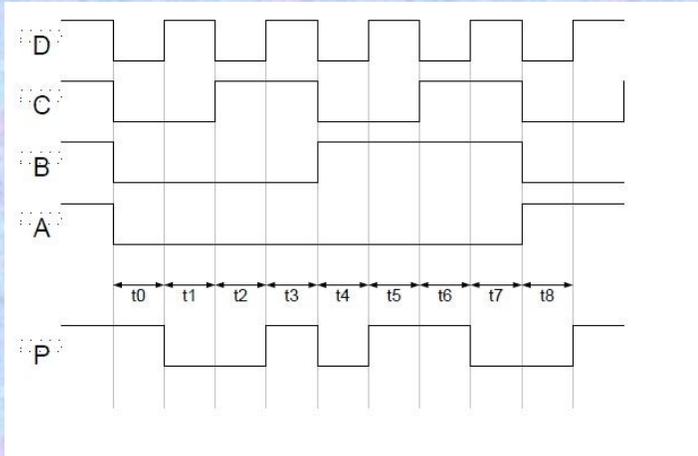
MIDTERM EXAMINATION 2010

Question No: 17 (Marks: 2)
For what values of A, B, C and D, value of the expression given below will be logic 1. Explain at least one combination.

$$\overline{A.\overline{B}} + \overline{\overline{A}.\overline{B}.C.D}$$

Answer:-
The Multiplexers are used to route the contents of any two registers to the ALU inputs. Many Audio signals in telephone network. Computer use Dynamic Memory addressing using same address line for row and column addressing to access data.

Question No: 18 (Marks: 2)
Provide some of the inputs for which the adjacent 1s detector circuit have active high output?
Answer:- (Page 123)
The Adjacent 1s Detector accepts 4-bit inputs.
If two adjacent 1s are detected in the input, the output is set to high.
 input combinations will be 0011, 0110, 0111, 1011, 1100, 1101, 1110 and 1111
The output function is a 1.

Question No: 19   (Marks: 2)
Draw the Truth-Table of NOR based S-R Latch
Answer:- (Page 222)

Input		Output
S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	invalid

Table 22.3   Truth-Table of NOR based S-R Latch

Question No: 20   (Marks: 3)
For a two bit comparator circuit specify the inputs for which A > B
Answer:- (Page 109)
The output A<B is set to 1 when the input combinations are 00 01, 00 10, 00 11, 01 10, 01 11 and 10 11

Question No: 21   (Marks: 3)
Draw the circuit diagram of NOR based S-R Latch ?
Answer:- (Page 220)
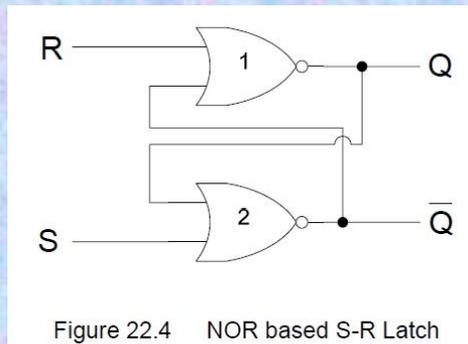
Figure 22.4   NOR based S-R Latch

Question No: 22   (Marks: 5)
One of the ABEL entry methods uses logic equations; explain it with at least a single example.
Answer: (Page 201)
ABEL however is case sensitive, thus variable 'A' is treated separately from variable 'a'. All ABEL equations must end with ';'.

Examples:-

(a) $X = A\bar{B}C + \overline{ABC} + AB + \bar{B}C$

(b) $Y = (\bar{A} + B + \bar{C} + D)(A + B + C)$

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Solution
(a)X = A& !B & C # !A & !B & !C # A & B # !B & C;
(b)Y = (!A # B # !C #D) & (A # B # C);

Question No: 23   (Marks: 5)
Explain Carry propagation in Parallel binary adder?
Answer: (Page 137)
Parallel Binary Adders can be implemented by connecting the required number of 1-bit full adders in a configuration represented in figure 14.9. However, there is a practical limitation to the number of 1-bit Full-Adders that can be connected in parallel. In the 4-bit Parallel Adder, the Most significant bit adder which adds bits A3, B3 and the Carry bit C3, cannot proceed until it receives the Carry from the next least significant 1-bit adder which adds bits A2, B2. The A2, B2 bit adder cannot precede unless it receives the carry input C2 from the A1, B1 adder. The A1, B1 adder in tern depends on A0, B0 adder to provide the carry input. Thus the carry has to propagate through each Full-adder before it reaches the last or most significant full adder.

MIDTERM EXAMINATION 2010

"Write the uses of multiplexer".   2 marks
Answer: (Page 167)
Multiplexer is a digital switch that has several inputs and a single output. Multiplexers are also known as Data Selectors. The main use of the Multiplexer is to select data from multiple sources and to route it to a single Destination

"Write any two advantages of Boolean expressions".   2 marks
Answer: (Page 71)
Boolean expressions which represent Boolean functions help in two ways. The function and operation of a Logic Circuit can be determined by Boolean expressions without implementing the Logic Circuit. Secondly, Logic circuits can be very large and complex. Such large circuits having many gates can be simplified and implemented using fewer gates.

"Draw the diagram of odd parity generator circuit".   2 marks
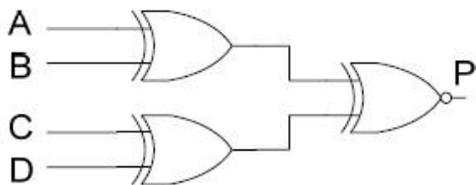**Answer: (Page 132)**

Figure 14.2   Odd-Parity Generator Circuit

"What does a 8-bit adder/subtracter circuit do"? 3 marks
Answer: (Page 146)
The Add/Subtract function select input are tied together. The Carry In of the 1_{st} 4-bit Adder circuit is connected to the Add/Subtract function select input. The Carry Out of the 1_{st} 4-bit Adder circuit is connected to the Carry In of the 2nd 4-bit Adder circuit.

"Draw the function table of 3 to 8 decoder".   3 marks
Answer: (Page 160)

Inputs						Outputs							
G1	G2A	G2B	C	B	A	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	1	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

"Describe 16 bit ALU".   5 marks
Answer: (Page 151)
The inputs A, B and the output F of the four, 4-bit ALUs 0, 1, 2 and 3 are connected to appropriate bits of the 16-bit inputs A, B and output F respectively. Thus bits A(0-3), B(0-3)and F(0-3) are connected to inputs and output of ALU0, bits A(4-7), B(4-7) and F(4-7) are connected to inputs and output of ALU1, bits A(8-11), B(8-11) and F(8-11) are connected to inputs and output of ALU2 and bits A(12-15), B(12-15) and F(12-15) are connected to inputs and output of ALU3. The Group-Carry Generate and Propagate outputs of the four ALUs are connected to the inputs of Look-Ahead Carry generator 74X182 respectively. The Carry outputs C1, C2 and C3 from the Look-Ahead Carry generator circuit are generated after a gate delay of 2 and are connected to the Carry in pins of ALUS 1, 2 and 3 respectively.

"Describe in your own words about latches".   5 marks
Answer: (repeated)

MIDTERM EXAMINATION 2009

Question No: 17   (Marks: 1)

Briefly state the basic principle of Repeated Division-by-2 method.
Answer: (Page 17)
Repeated Division-by-2 method allows decimal numbers of any magnitude to be converted into binary.

Question No: 18   (Marks: 1)
Briefly state the basic principle of Repeated Multiplication-by-2 Method.
Answer: Page 17
Repeated Multiplication-by-2 method allows decimal fractions of any magnitude to be easily converted into binary.

Question No: 19   (Marks: 2)
Draw the circuit diagram of a Tri-State buffer.
Answer: (Repeated)

Question No: 20   (Marks: 3)
Add -13 and +7 by converting them in binary system your result must be in binary.

Question No: 21   (Marks: 5)
Explain "Sum of Weights" method with example for "Octal to Decimal" conversion
Answer: (Page 14) (Page 33)
In the Sum-of-Weights method an extended expression is written in terms of the Binary Base Number 2 and the weights of the Binary number to be converted. The weights correspond to each of the binary bits which are multiplied by the corresponding binary value.Binary bits having the value 0 do not contribute any value towards the final sum expression.

An Octal number can be directly converted into Decimal by using the sum of weights method. The conversion steps using the Sum-of-Weights method are shown.

4033	Octal number
$4 \times 8^3 + 0 \times 8^2 + 3 \times 8^1 + 3 \times 8^0$	Writing the number in an expression
$(4 \times 512) + (0 \times 64) + (3 \times 8) + (3 \times 1)$	
$2048 + 0 + 24 + 3$	Summing the Weights
2075	Decimal equivalent

Question No: 22   (Marks: 10)
Explain the Implementation of an Odd-Parity Generator Circuit i.e by drawing function table, maping it to K-map and then simplifying the expression.

<p align="center">**MIDTERM EXAMINATION 2009**</p>

Question No: 17   (Marks: 1)

Briefly state the basic principle of Repeated Multiplication-by-2 Method.
Answer: (Repeated)

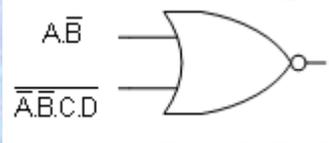**Question No: 18   (Marks: 1)**

How standard Boolean expressions can be converted into truth table format.
Answer: (Page 87)
All standard Boolean expressions can be easily converted into truth table format using binary values for each term in the expression. Standard SOP or POS expressions can also be determined from a truth table.

Question No: 19   (Marks: 2)

What will be the out put of the diagram given below

Question No: 20   (Marks: 3)
When an Input (source) file is created in ABEL a module is created which has three sections. Name
These three sections.
Answer: (Page 205)
    1. Declarations
    2. Logic Descriptions
    3. Test Vectors

Question No: 21   (Marks: 5)
Explain "AND" Gate and some of its uses
Answer: (Page 40)
The AND Gate performs a logical multiplication function. An AND Gate has multiple inputs and a single output. Most commonly used AND Gates are two input AND gates.
An important use of an AND gate in addition to the multiplication operation is its use to disable or enable a device. Counter device counts from 0 to 100. The counter device increments its current count value to the next when it receives a pulse at its clock input.

Question No: 22   (Marks: 10)

Write down different situations where we need the sequential circuits.
Answer: (Page 217)
This type of system uses storage elements called flip-flops that are employed to change their binary value only at discrete instants of time. Synchronous sequential circuits use logic gates and flip-flop storage devices. Sequential circuits have a clock signal as one of their inputs. All state transitions in such circuits occur only when the clock value is either 0 or 1 or happen at the rising or falling edges of the clock depending on the type of memory elements used in the circuit.

MIDTERM EXAMINATION 2009

Question No: 17   (Marks: 1)
How can a PLD be programmed?
Answer: (Page 194)
PLDs are programmed with the help of computer which runs the programming software. The computer is

connected to a programmer socket in which the PLD is inserted for programming. PLDs can also be programmed when they are installed on a circuit board

Question No: 18   (Marks: 1)
How many input and output bits do a Half-Adder contain?
Answer: (Page 134):
The Half-Adder has a 2 input bits and 2 output bits.

Question No: 19   (Marks: 2)
Explain the difference between 1-to-4 Demultiplexer 2-to-4 Binary Decoder?
Answer: (Page 178)
The circuit of the 1-to-4 Demultiplexer is similar to the 2-to-4 Binary Decoder. The only difference between the two is the addition of the Data Input line, which is used as enable line in the 2-to-4 Decoder circuit.

Question No: 20   (Marks: 3)
Name the three declarations that are included in "declaration section" of the module that is created when an Input (source) file is created in ABEL.
Answer: (repeated)

Question No: 21   (Marks: 5)
Explain with example how noise affects Operation of a CMOS AND Gate circuit.
Answer: (Page 123)
Two CMOS 5 volt series AND gates are connected together. Figure 7.3 The first AND gate has both its inputs connected to logic high, therefore the output of the gate is guaranteed to be logic high. The logic high voltage output of the first AND gate is assumed to be 4.6 volts well within the valid VOH range of 5-4.4 volts. Assume the same noise signal (as described earlier) is added to the output signal of the first AND gate.

Question No: 22   (Marks: 10)
Explain the SOP based implementation of the Adjacent 1s Detector Circuit
Answer: (Page 123)

The Adjacent 1s Detector accepts 4-bit inputs. If two adjacent 1s are detected in the input, the output is set to high. The operation of the Adjacent 1s Detector is represented by the function table. Table 13.6. In the function table, for the input combinations 0011, 0110, 0111, 1011, 1100, 1101, 1110 and 1111 the output function is a 1.

Implementing the circuit directly from the function table based on the SOP form requires 8 AND gates for the 8 product terms (minterms) with an 8-input OR gate. Figure 13.3. The total gate count is
   • One 8 input OR gate
   • Eight 4 input AND gates
   • Ten NOT gates
The expression can be simplified using a Karnaugh map, figure 13.4, and then the simplified expression can be implemented to reduce the gate count. The simplified expression is $AB + CD + BC$. The circuit implemented using the expression $AB + CD + BC$ has reduced to 3 input OR gate and 2 input AND gates. Figure 13.5

Question No: 17   (Marks: 1)
Which device performs an operation which is the opposite of the Decoder function?
Answer: (Page 163)
An Encoder functional device performs an operation which is the opposite of the Decoder function.

Question No: 18   (Marks: 1)
Name any two modes in which PALs are programmed.
Answer: (Page 199)
The three modes in which PALs are programmed are
• Simple
• Complex
• Registered

Question No: 19   (Marks: 2)
Explain Combinational Function Devices?
Answer: (Page 133)
Digital circuits are formed by the combination of Logic Gates. Xor, Xnor, NAND, NOR are combinational function devices.

Question No: 20   (Marks: 3)
Differentiate between hexadecimal and octal number system
Answer:
Octa decimal use Base 8 whereas Hexa decimal use Base 16

Question No: 21   (Marks: 5)
Explain "Sum-of-Weights Method" for Hexadecimal to Decimal Conversion with at least one example?
Answer:
The hexadecimal (Hex) numbering system provides even shorter notation than octal. Hexadecimal uses a base of 16. It employs 16 digits: number 0 through 9, and letters A through F, with A through F substituted for numbers 10 to 15, respectively,
Hexadecimal numbers can be expressed as their decimal equivalents by using the sum of weights method, as shown in the following example:

```
     Weight        2     1     0
     Hex. Number   1     B     7
```

$$7 \times 16^0 = 7 \times 1 \ = \ 7$$
$$11 \times 16^1 = 11 \times 16 \ = \ 176$$
$$1 \times 16^2 = 1 \times 256 = \ 256$$

Sum of products 439_{10}

Like octal numbers, hexadecimal numbers can easily be converted to binary or vise versa. Conversion is accomplished by writing the 4-bit binary equivalent of the hex digit for each position, as illustrated in the following example:

Hex. Number   1   B   7

0001   1011   0111   ←   Binary number

Hexadecimal	Binary	Decimal
0	0000	0
1	**0001**	**1**
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	**0111**	**7**
8	1000	8
9	1001	9
A	1010	10
B	**1011**	**11**
C	1100	12
D	1101	13
E	1110	14
F	1111	15

Question No: 22   (Marks: 10)
Draw the function table of two-bit comparator circuit, map it to K-Map and derive the expression for (A > B)
Answer: (Page 109)

Input				Output		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1

0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0