**Set- A**

**Rajasthan Institute of Engineering & Technology, Jaipur.**

**I Mid Term examination**

**Session: 2018-19**

**B. Tech. VII Sem & Branch: Electronics & Communication Engineering**

**Subject with code: 7EC5A VLSI Design**

Time: 2 hrs. M.M.:20

**Instruction for students:**

1. No provision for supplementary answer book.
2. All questions carry equal marks.

Q.1 Explain the structure and operation of MOS transistor.

Or

Q.1 Explain memory latches and registers in CMOS logic circuits.

Q.2 Define Enhancement mode transistor action by drawing its working diagram.

Or

Q.2 Explain transmission gates by drawing its appropriate diagrams.

Q.3 Define CMOS inverter and explain its working with diagrams.

Or

Q.3 What do you mean by high order effect in MOSFET.

Q.4 Discuss following High Order effects in MOSFET:

(i) Narrow Channel effect (ii) Sub threshold conduction.

Or

Q.4 Write short notes on 2 inputs CMOS Multiplexer.

**Set- B**

**Rajasthan Institute of Engineering & Technology, Jaipur.**

**I Mid Term examination**

**Session: 2018-19**

**B. Tech. VII Sem & Branch: Electronics & Communication Engineering**

**Subject with code: 7EC5A VLSI Design**

Time: 2 hrs. M.M.:20

**Instruction for students:**

1. No provision for supplementary answer book.
2. All questions carry equal marks.

Q.1 Describe about basic MOS transistor by drawing its n-MOS and p-MOS enhancement mode transistors.

Or

Q.1 Describe estimation of gate delays in CMOS.

Q.2 What do you mean by CMOS logic inverter and give its processing by its diagrams.

Or

Q.2 Derive pull up to pull down ratio for a NMOS inverter and CMOS inverter (βn/βp).

Q.3 Explain designing of NAND and NOR gate.

Or

Q.3 Write short notes on channel length modulation.

Q.4 Explain noise margin in CMOS inverter.

Or

Q.4 Explain the fabrication process of MOSFET using self-aligned poly gate technology.