**SET B**

University Roll No: -------------------------

**RAJASTHAN INSTITUTE OF ENGINEERING & TECHNOLOGY JAIPUR, RAJASTHAN**

**B. Tech. II Midterm EXAMINATION 2017-18**

**Semester and Branch**: III Year, VI Semester, EE

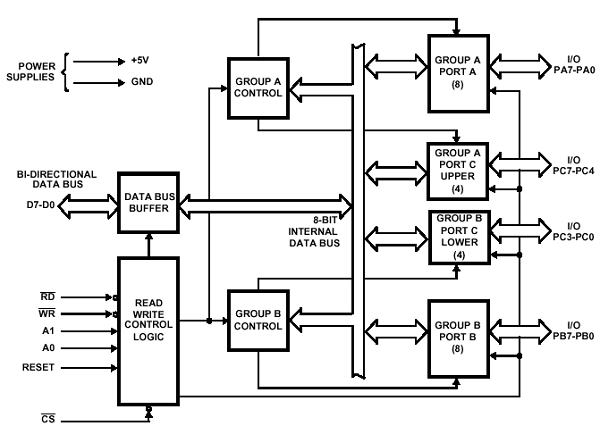
**Subject:** Advanced Microprocessor

***Duration*: Hours             *Maximum Marks*: 20**

**Student Instructions:**

* **All questions are compulsory.**
* **All questions carry equal marks.**
* **Use pencils for the diagrams.**

**Q.1 Explain the Architecture of 8255A programmable peripheral Interface Chip.**



The 8255A is a general purpose programmable I/O device designed to transfer the data from I/O to interrupt I/O under certain conditions as required. It can be used with almost any microprocessor.

It consists of three 8-bit bidirectional I/O ports (24I/O lines) which can be configured as per the requirement.

## Ports of 8255A

8255A has three ports, i.e., PORT A, PORT B, and PORT C.

* Port A contains one 8-bit output latch/buffer and one 8-bit input buffer.
* Port B is similar to PORT A.
* Port C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word.

These three ports are further divided into two groups, i.e. Group A includes PORT A and upper PORT C. Group B includes PORT B and lower PORT C. These two groups can be programmed in three different modes, i.e. the first mode is named as mode 0, the second mode is named as Mode 1 and the third mode is named as Mode 2.

## Operating Modes

8255A has three different operating modes −

* Mode 0 − In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports. Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched. Ports do not have interrupt capability.
* Mode 1 − In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either input or output ports. Each port uses three lines from port C as handshake signals. Inputs and outputs are latched.
* Mode 2 − In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

## Features of 8255A

The prominent features of 8255A are as follows −

* It consists of 3 8-bit IO ports i.e. PA, PB, and PC.
* Address/data bus must be externally demux'd.
* It is TTL compatible.
* It has improved DC driving capability.

OR

**Q.1 Explain the Features of 8259A Programmable Interrupt Controller Chip.**

Ans:

**Features:**

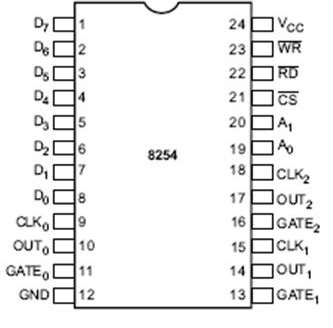
1. It is a LSI chip which manages 8 levels of interrupts i.e. it is used to implement 8 level interrupt systems.
2. It can be cascaded in a master slave configuration to handle up to 64 levels of interrupts.
3. It can identify the interrupting device.
4. It can resolve the priority of interrupt requests i.e. it does not require any external priority resolver.
5. It can be operated in various priority modes such as fixed priority and rotating priority.
6. The interrupt requests are individually mask-able.
7. The operating modes and masks may be dynamically changed by the software at any time during execution of programs.
8. It accepts requests from the peripherals, determines priority of incoming request, checks whether the incoming request has a higher priority value than the level currently being serviced and issues an interrupt signal to the microprocessor.
9. It provides 8 bit vector number as an interrupt information.
10. It does not require clock signal.
11. It can be used in polled as well as interrupt modes.
12. The starting address of vector number is programmable.
13. It can be used in buffered mode.

**Q.2 Explain the PIN Diagram of 8253A timer chip.**

**Ans:**

## 8254 Pin Description

Here is the pin diagram of 8254 −



In the above figure, there are three counters, a data bus buffer, Read/Write control logic, and a control register. Each counter has two input signals - CLOCK & GATE, and one output signal - OUT.

### Data Bus Buffer

It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus. It has three basic functions −

* Programming the modes of 8253/54.
* Loading the count registers.
* Reading the count values.

### Read/Write Logic

It includes 5 signals, i.e. RD, WR, CS, and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW.

Address lines A0 & A1 of the CPU are connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 & A1.

|  |  |  |
| --- | --- | --- |
| A1 | A0 | Result |
| 0 | 0 | Counter 0 |
| 0 | 1 | Counter 1 |
| 1 | 0 | Counter 2 |
| 1 | 1 | Control Word Register |
| X | X | No Selection |

### Control Word Register

This register is accessed when lines A0 & A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation. Following table shows the result for various control inputs.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A1 | A0 | RD | WR | CS | Result |
| 0 | 0 | 1 | 0 | 0 | Write Counter 0 |
| 0 | 1 | 1 | 0 | 0 | Write Counter 1 |
| 1 | 0 | 1 | 0 | 0 | Write Counter 2 |
| 1 | 1 | 1 | 0 | 0 | Write Control Word |
| 0 | 0 | 0 | 1 | 0 | Read Counter 0 |
| 0 | 1 | 0 | 1 | 0 | Read Counter 1 |
| 1 | 0 | 0 | 1 | 0 | Read Counter 2 |
| 1 | 1 | 0 | 1 | 0 | No operation |
| X | X | 1 | 1 | 0 | No operation |
| X | X | X | X | 1 | No operation |

### Counters

Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output is configured by the selection of modes stored in the control word register. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

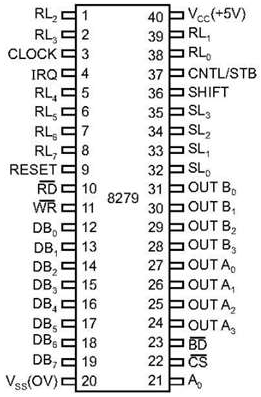
OR

**Q.2 Explain the PIN Diagram of Keyboard/Display Controller 8279A Chip.**

Ans:

### 8279 − Pin Description

The following figure shows the pin diagram of 8279 −



### Data Bus Lines, DB0 - DB7

These are 8 bidirectional data bus lines used to transfer the data to/from the CPU.

### CLK

The clock input is used to generate internal timings required by the microprocessor.

### RESET

As the name suggests this pin is used to reset the microprocessor.

### CS Chip Select

When this pin is set to low, it allows read/write operations, else this pin should be set to high.

### A0

This pin indicates the transfer of command/status information. When it is low, it indicates the transfer of data.

### RD, WR

This Read/Write pin enables the data buffer to send/receive data over the data bus.

### IRQ

This interrupt output line goes high when there is data in the FIFO sensor RAM. The interrupt line goes low with each FIFO RAM read operation. However, if the FIFO RAM further contains any key-code entry to be read by the CPU, this pin again goes high to generate an interrupt to the CPU.

### Vss, Vcc

These are the ground and power supply lines of the microprocessor.

### SL0 − SL3

These are the scan lines used to scan the keyboard matrix and display the digits. These lines can be programmed as encoded or decoded, using the mode control register.

### RL0 − RL7

These are the Return Lines which are connected to one terminal of keys, while the other terminal of the keys is connected to the decoded scan lines. These lines are set to 0 when any key is pressed.

### SHIFT

The Shift input line status is stored along with every key code in FIFO in the scanned keyboard mode. Till it is pulled low with a key closure, it is pulled up internally to keep it high

### CNTL/STB - CONTROL/STROBED I/P Mode

In the keyboard mode, this line is used as a control input and stored in FIFO on a key closure. The line is a strobe line that enters the data into FIFO RAM, in the strobed input mode. It has an internal pull up. The line is pulled down with a key closure.

### BD

It stands for blank display. It is used to blank the display during digit switching.

### OUTA0 – OUTA3 and OUTB0 – OUTB3

These are the output ports for two 16x4 or one 16x8 internal display refresh registers. The data from these lines is synchronized with the scan lines to scan the display and the keyboard.

## Operational Modes of 8279

There are two modes of operation on 8279 − **Input Mode** and **Output Mode**.

### Input Mode

This mode deals with the input given by the keyboard and this mode is further classified into 3 modes.

* **Scanned Keyboard Mode** − In this mode, the key matrix can be interfaced using either encoded or decoded scans. In the encoded scan, an 8×8 keyboard or in the decoded scan, a 4×8 keyboard can be interfaced. The code of key pressed with SHIFT and CONTROL status is stored into the FIFO RAM.
* **Scanned Sensor Matrix** − In this mode, a sensor array can be interfaced with the processor using either encoder or decoder scans. In the encoder scan, 8×8 sensor matrix or with decoder scan 4×8 sensor matrix can be interfaced.
* **Strobed Input** − In this mode, when the control line is set to 0, the data on the return lines is stored in the FIFO byte by byte.

### Output Mode

This mode deals with display-related operations. This mode is further classified into two output modes.

* **Display Scan** − This mode allows 8/16 character multiplexed displays to be organized as dual 4-bit/single 8-bit display units.
* **Display Entry** − This mode allows the data to be entered for display either from the right side/left side.

**Q.3 Explain the Features of DMA Controller.**

Ans:

DMA stands for Direct Memory Access. It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the data directly to/from memory without any interference of the CPU.

Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so the device is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

How DMA Operations are Performed?

Following is the sequence of operations performed by a DMA −

* Initially, when any device has to send data between the device and the memory, the device has to send DMA request (DRQ) to DMA controller.
* The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assert the HLDA.
* Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPU leaves the control over bus and acknowledges the HOLD request through HLDA signal.
* Now the CPU is in HOLD state and the DMA controller has to manage the operations over buses between the CPU, memory, and I/O devices.

Features of 8257

Here is a list of some of the prominent features of 8257 −

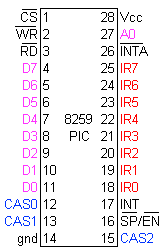
* It has four channels which can be used over four I/O devices.
* Each channel has 16-bit address and 14-bit counter.
* Each channel can transfer data up to 64kb.
* Each channel can be programmed independently.
* Each channel can perform read transfer, write transfer and verify transfer operations.
* It generates MARK signal to the peripheral device that 128 bytes have been transferred.
* It requires a single phase clock.
* Its frequency ranges from 250Hz to 3MHz.
* It operates in 2 modes, i.e., Master mode and Slave mode.

**OR**

**Q.3 Explain the PIN Diagram of 8259A Programmable Interrupt Controller Chip.**

**Features:**

* 8 levels of interrupts.
* Can be cascaded in master-slave configuration to handle 64 levels of interrupts.
* Internal priority resolver.
* Fixed priority mode and rotating priority mode.
* Individually maskable interrupts.
* Modes and masks can be changed dynamically.
* Accepts IRQ, determines priority, checks whether incoming priority > current level being serviced, issues interrupt signal.
* In 8085 mode, provides 3 byte CALL instruction. In 8086 mode, provides 8 bit vector number.
* Polled and vectored mode.
* Starting address of ISR or vector number is programmable.
* No clock required.



|  |  |
| --- | --- |
| D0-D7 | Bi-directional, tristated, buffered data lines. Connected to data bus directly or through buffers |
| RD-bar | Active low read control |
| WR-bar | Active low write control |
| A0 | Address input line, used to select control register |
| CS-bar | Active low chip select |
| CAS0-2 | Bi-directional, 3 bit cascade lines. In master mode, PIC places slave ID no. on these lines. In slave mode, the PIC reads slave ID no. from master on these lines. It may be regarded as slave-select. |
| SP-bar / EN-bar | Slave program / enable. In non-buffered mode, it is SP-bar input, used to distinguish master/slave PIC. In buffered mode, it is output line used to enable buffers |
| INT | Interrupt line, connected to INTR of microprocessor |
| INTA-bar | Interrupt ack, received active low from microprocessor |
| IR0-7 | Asynchronous IRQ input lines, generated by peripherals. |

**Q.4 What is the means of Digital to Analog Converter? Explain with the help of Digital to Analog Converter Chip.**

**Ans**

An analog-to-digital converter, or ADC as it is more commonly called, is a [device](https://www.webopedia.com/TERM/D/device.html) that converts [analog](https://www.webopedia.com/TERM/A/analog.html) signals into [digital](https://www.webopedia.com/TERM/D/digital.html) signals. Analog information is transmitted by modulating a continuous transmission signal by amplifying a signal's strength or varying its frequency to add or take away data. Digital information describes any system based on discontinuous data or events. [Computers](https://www.webopedia.com/TERM/C/computer.html), which handle data in digital form, require analog-to-digital converters to turn signals from analog to digital before it can be read. One example is a [modem](https://www.webopedia.com/TERM/M/modem.html) which turns signals from digital to analog before transmitting those signals over communication lines such as telephone lines that carry only analog signals. The signals are turned back into digital form ([demodulated](https://www.webopedia.com/TERM/M/modulate.html)) at the receiving end so that the computer can process the [data](https://www.webopedia.com/TERM/D/data.html) in its digital format.



The AD7523 and AD7533 monolithic, low cost, high performance, 8-bit and 10-bit accurate, multiplying digital-to-analog converter (DAC), in a 16 pin DIP. Harris’ thin film resistors on CMOS circuitry provide 10-bit resolution (8, 9 and 10-bit accuracy), with TTL/CMOS compatible operation. The AD7523 and AD7533s accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter. Low noise audio gain controls, motor speed controls, digitally controlled gain and digital attenuators are a few of the wide range of applications of the AD7523 and AD7533.

**OR**

**Q.4 Explain the Architecture of 8087 Numeric data processor**

Ans:

8087 numeric data processor is also known as **Math co-processor, Numeric processor extension** and **Floating point unit**. It was the first math coprocessor designed by Intel to pair with 8086/8088 resulting in easier and faster calculation.

Once the instructions are identified by the 8086/8088 processor, then it is allotted to the 8087 co-processor for further execution.

The data types supported by 8087 are −

* Binary Integers
* Packed decimal numbers
* Real numbers
* Temporary real format

The most prominent features of 8087 numeric data processor are as follows −

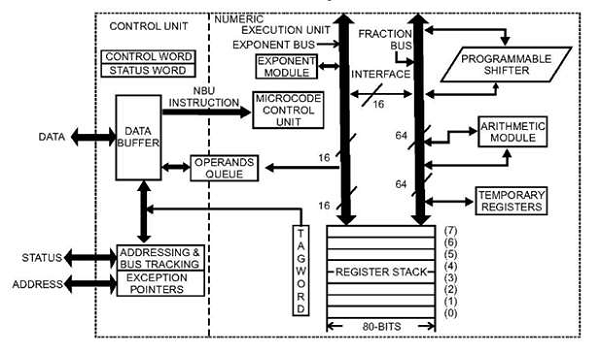
* It supports data of type integer, float, and real types ranging from 2-10 bytes.
* The processing speed is so high that it can calculate multiplication of two 64-bits real numbers in ~27 µs and can also calculate square-root in ~35 µs.
* It follows IEEE floating point standards.

8087 Architecture

8087 Architecture is divided into two groups, i.e., **Control Unit** (CU) and **Numeric Extension Unit** (NEU).

* The **control unit** handles all the communication between the processor and the memory such as it receives and decodes instructions, reads and writes memory operands, maintains parallel queue, etc. All the coprocessor instructions are ESC instructions, i.e., they start with ‘F’, the coprocessor only executes the ESC instructions while other instructions are executed by the microprocessor.
* The **numeric extension unit** handles all the numeric processor instructions like arithmetic, logical, transcendental, and data transfer instructions. It has 8 register stack, which holds the operands for instructions and their results.

The architecture of 8087 coprocessor is as follows −



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